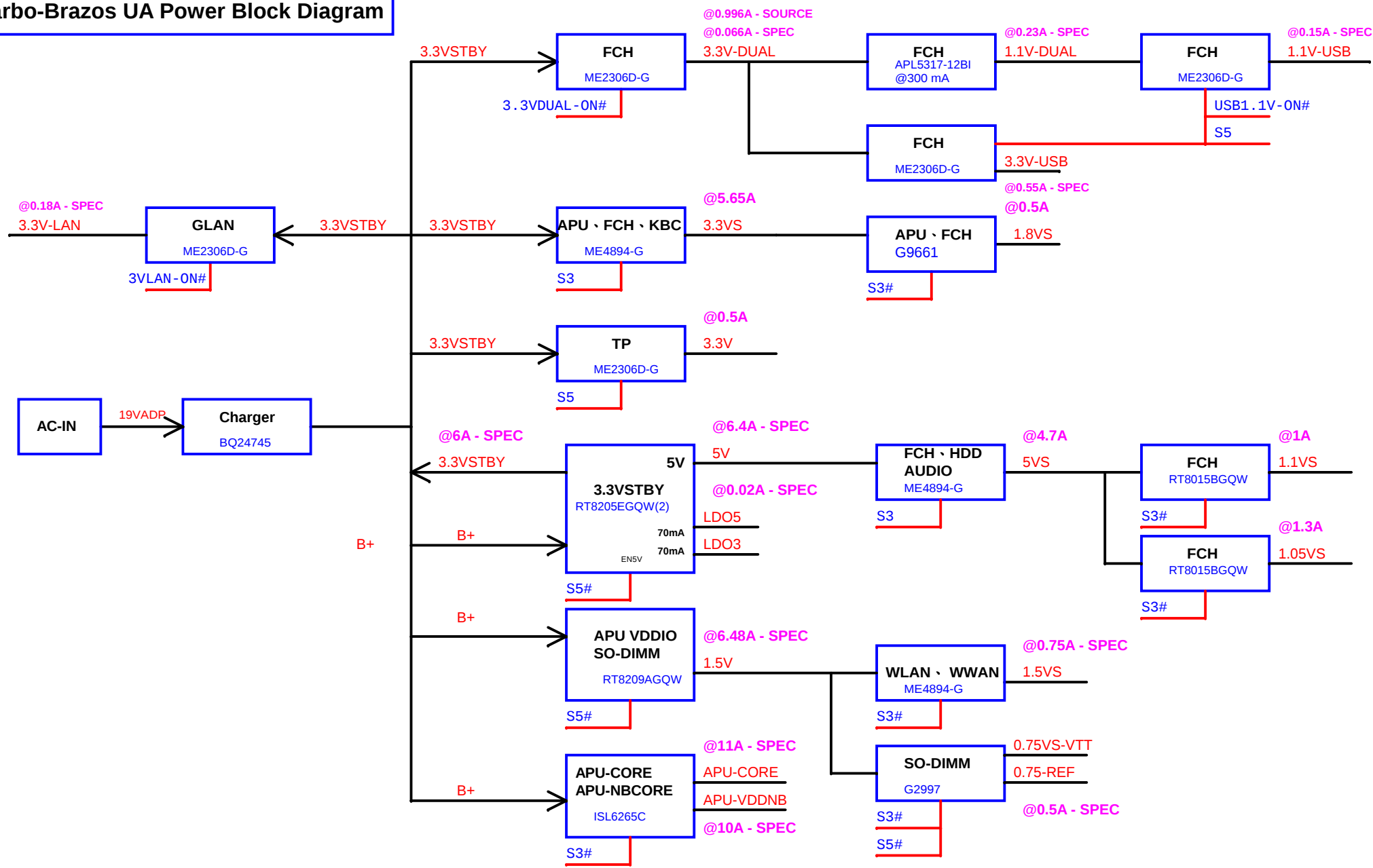


Garbo-Brazos UA Power Block Diagram



APU_MEMORY/PCIE/UMI

U506E

ONTARIO (2.0) PART 1 OF 5

U506A

ONTARIO (2.0) PART 2 OF 5

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

Place close APU pin M23

FLEX Computing

Project Name : H210UA1 Title : APU_MEMORY/PCIE/UMI

Size : Document Number : HPMH-40GAB6000-C000 Rev : C

Date : Monday, September 27, 2010 Sheet : 3 of 28

APU_MEMORY/PCIE/UMI

U06E

U06A

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

Place close APU pin M23

FLEX Computing

Project Name : **H210UA1** Title : **APU_MEMORY/PCIE/UMI**

Size : Document Number : **HPMH-40GAB6000-C000** Rev : **C**

Date : Monday, September 27, 2010 Sheet : 3 of 28

APU_MEMORY/PCIE/UMI

U06E

U06A

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

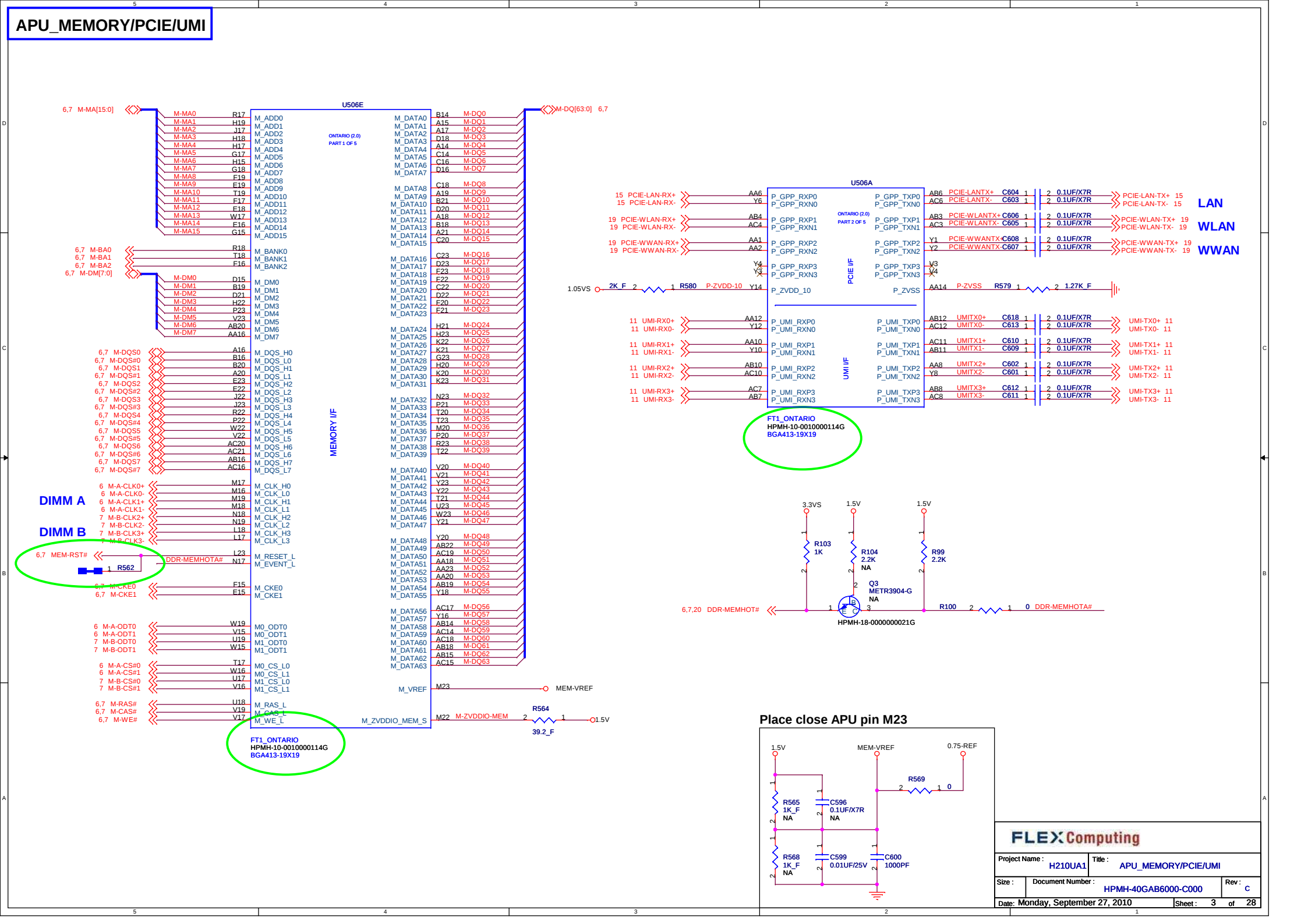
Place close APU pin M23

FLEX Computing

Project Name : **H210UA1** Title : **APU_MEMORY/PCIE/UMI**

Size : Document Number : **HPMH-40GAB6000-C000** Rev : **C**

Date : Monday, September 27, 2010 Sheet : 3 of 28



APU_MEMORY/PCIE/UMI

U06E

U06A

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

FT1_ONTARIO
HPMH-10-0010000114G
BG4A13-19X19

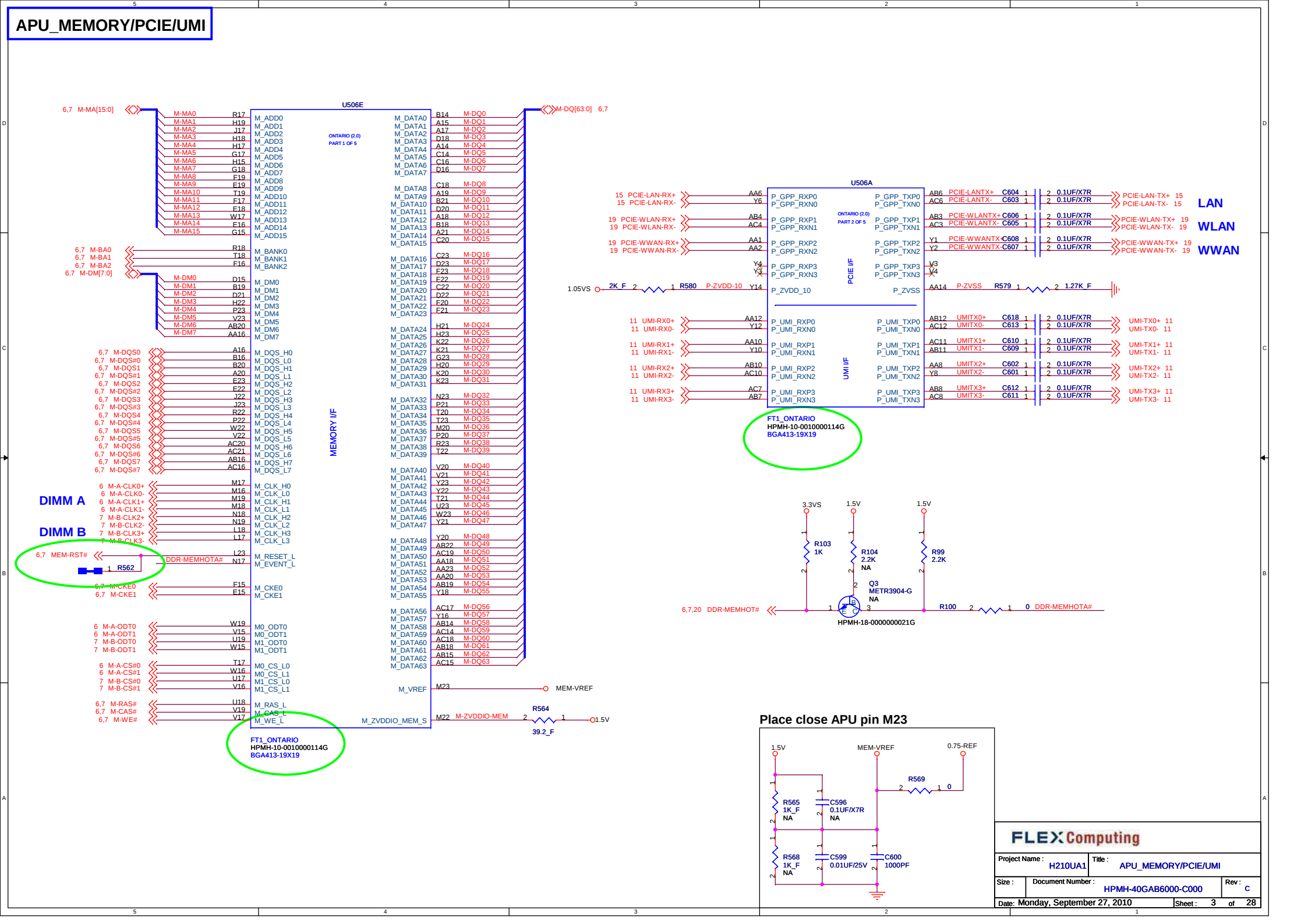
Place close APU pin M23

FLEX Computing

Project Name : **H210UA1** Title : **APU_MEMORY/PCIE/UMI**

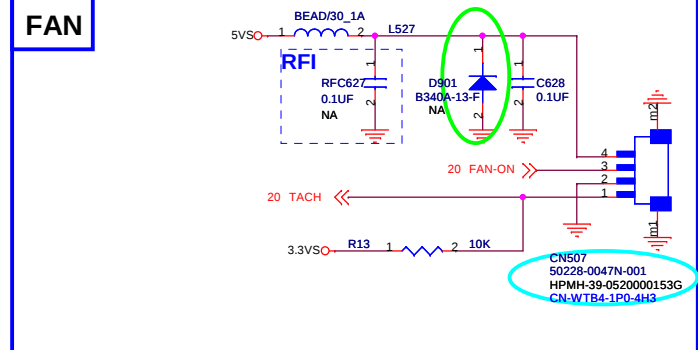
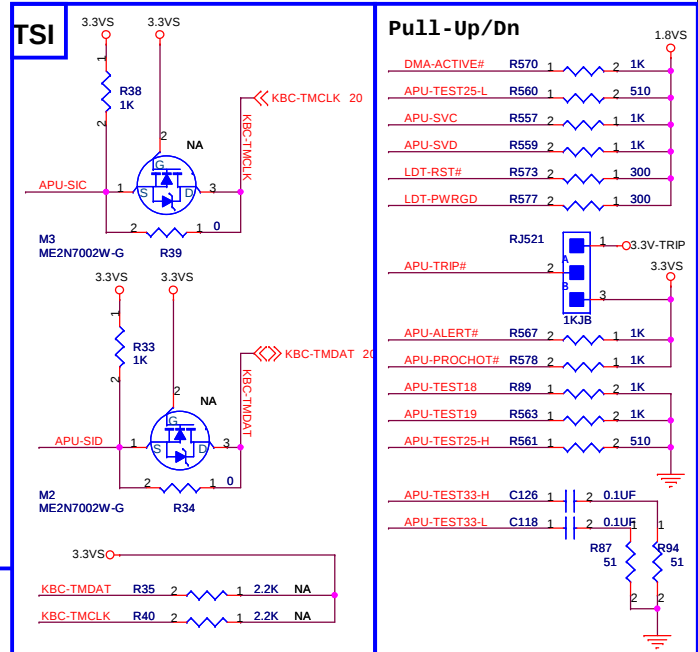
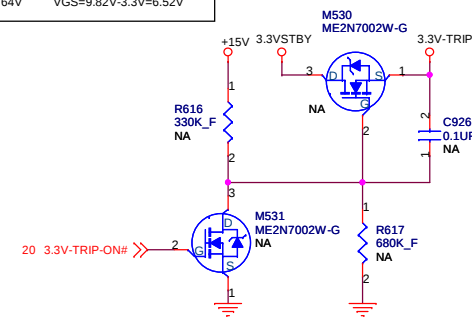
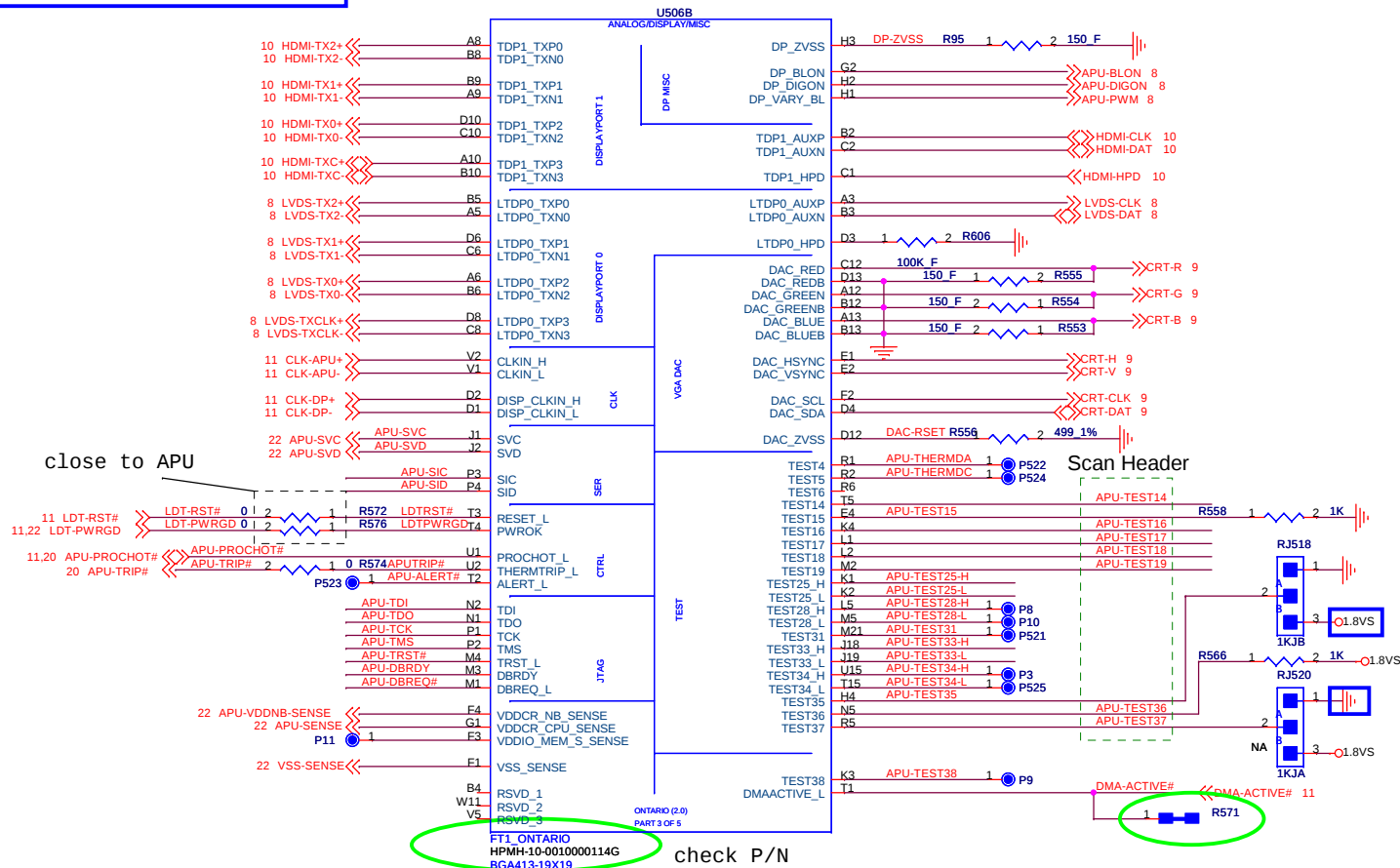
Size : Document Number : **HPMH-40GAB6000-C000** Rev : **C**

Date : Monday, September 27, 2010 Sheet : 3 of 28



APU_DISPLAY/CLK/MISC

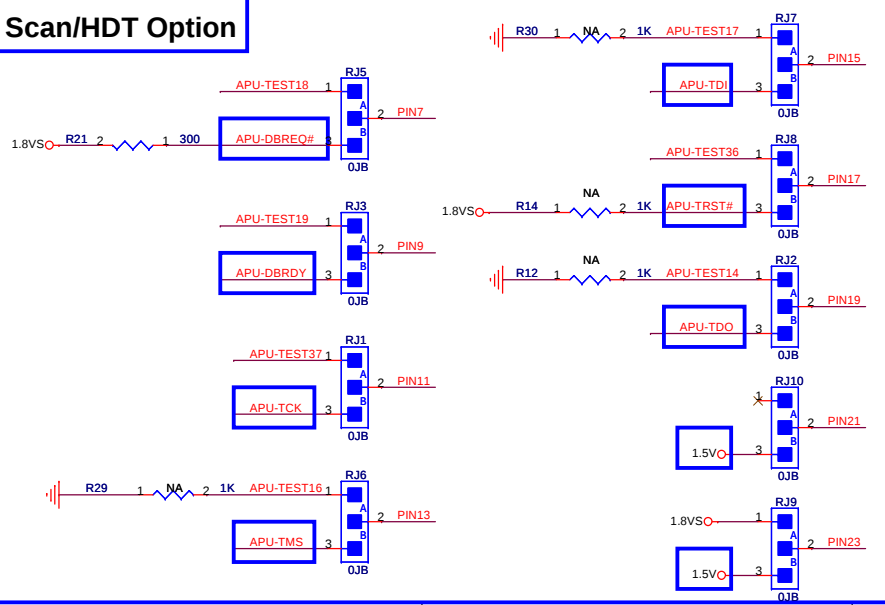
ME2N7002W-G VGS=1(min) ~ 2.5(max)	
+15= 11.8V ,VG=7.94V	+15= 14.6V ,VG=9.82V
VGS=7.94V-3.3V=4.64V	VGS=9.82V-3.3V=6.52V



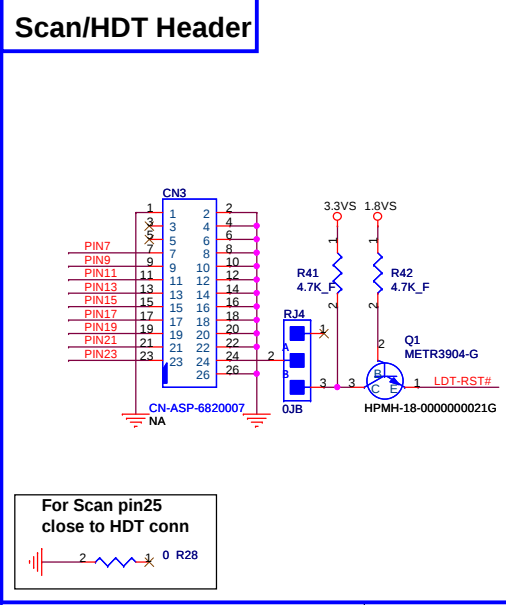
FLEX Computing

Project Name : H210UA1		Title : APU_DISPLAY/CLK/MISC	
Size :	Document Number : HPMH-40GAB6000-C000		Rev : C
Date: Monday, September 27, 2010		Sheet : 4 of 28	

Scan/HDT Option

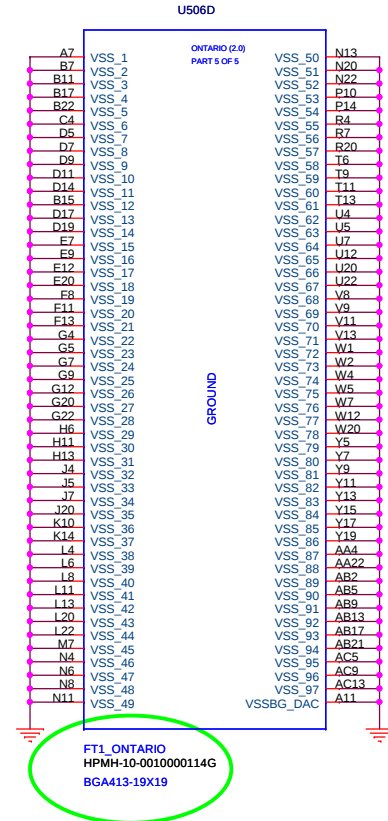
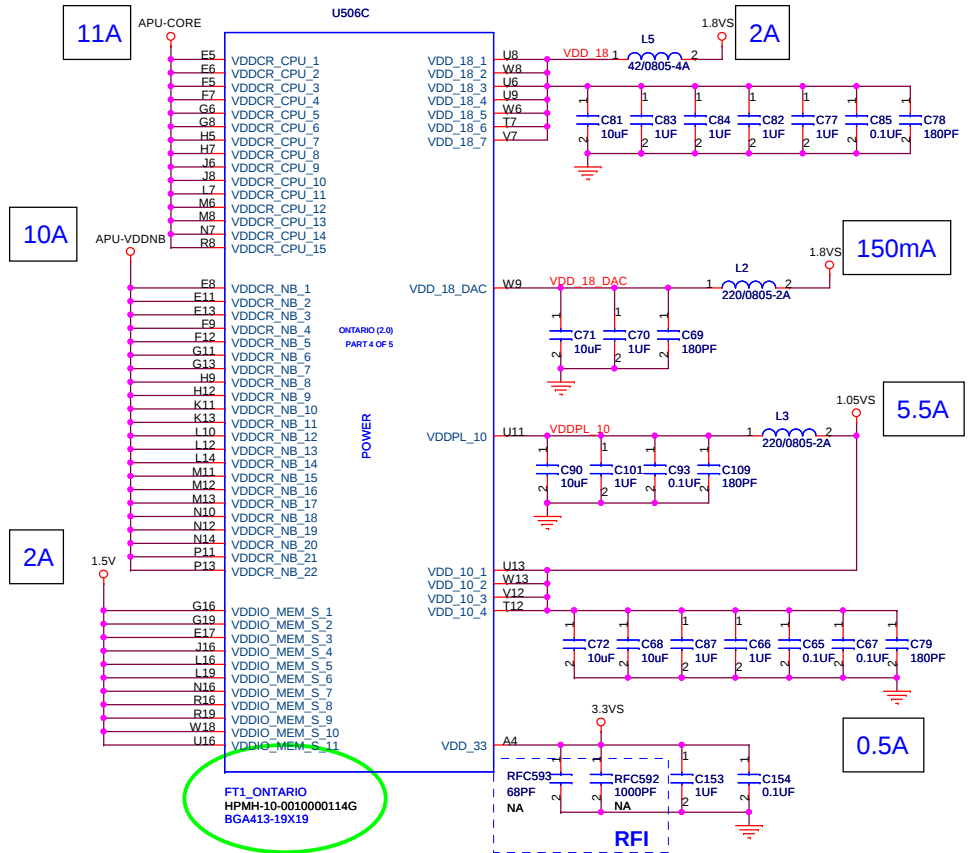


Scan/HDT Header

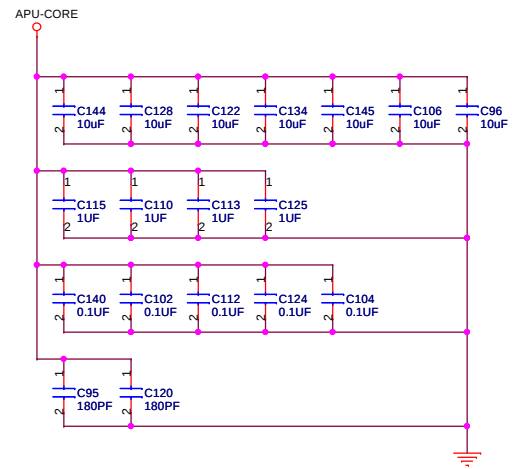


For Scan pin25
close to HDT conn

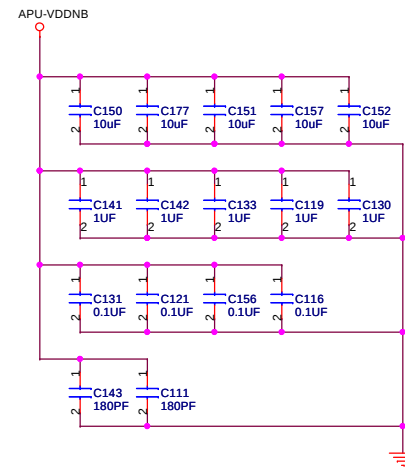
APU_POWER & GND



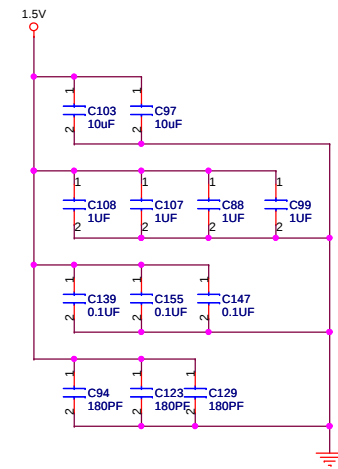
For APU-CORE



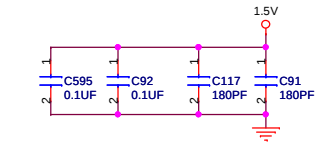
For APU-VDDNB



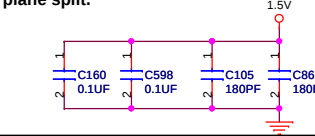
For 1.5V



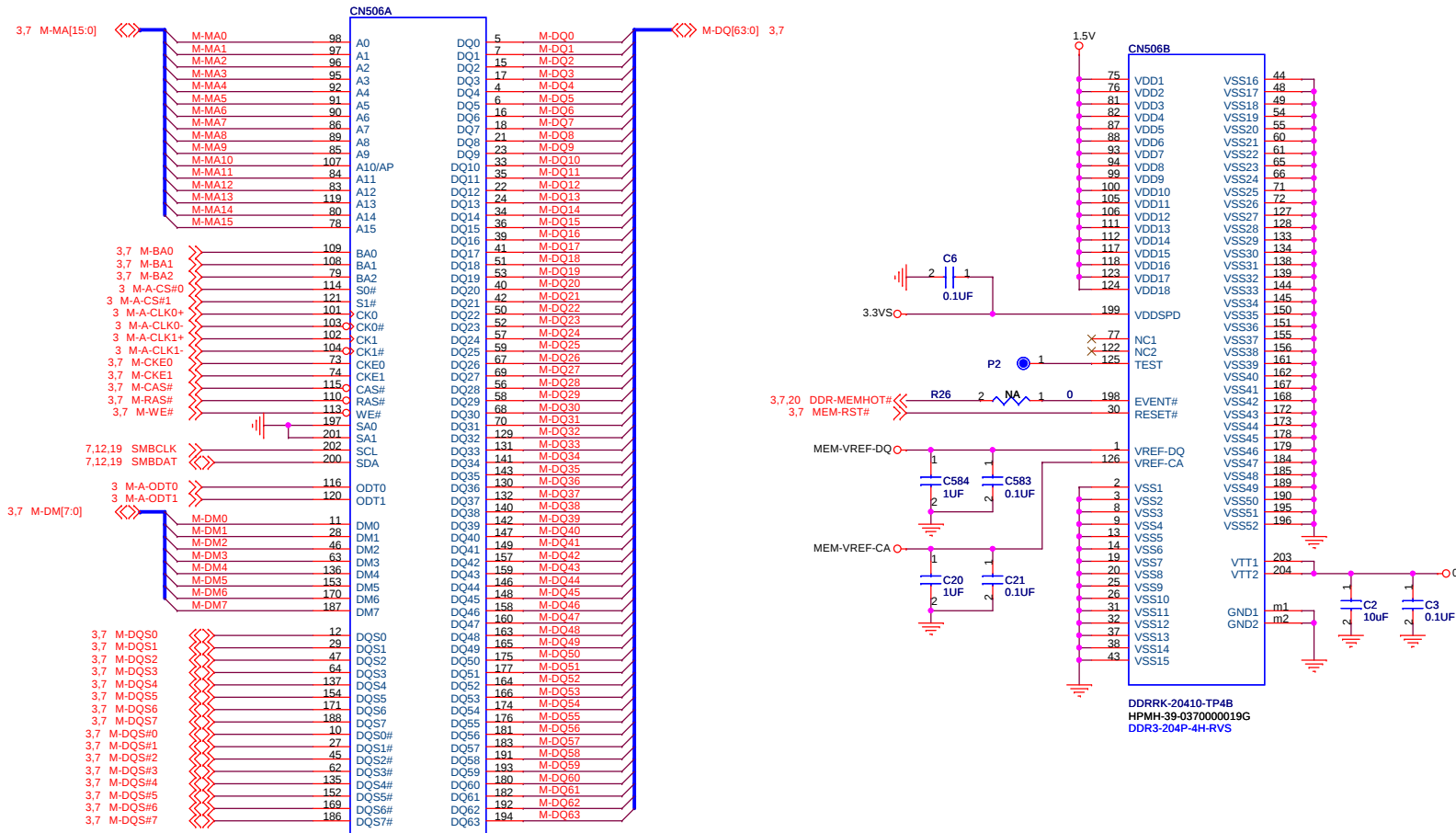
If the VSS plane is cut to create a VDDIO_MEM_S plane, ceramic capacitors are connected across the VDDIO_MEM_S and VSS plane split.



If the VSS plane is longer than 63.5 mm an additional two capacitors are required across the VDDIO_MEM_S and VSS plane split.



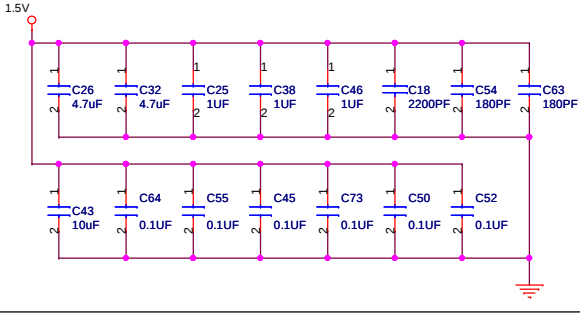
DDR3 DIMM A



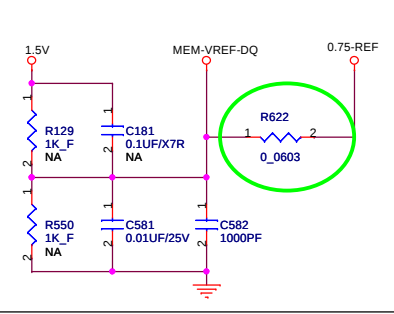
SA0	SA1	Address
0	0	A0
1	0	A2

DDRRK-20410-TP4B
HPMH-39-0370000019G
DDR3-204P-4H-RVS

Layout :
Place these Caps near So-DimmA



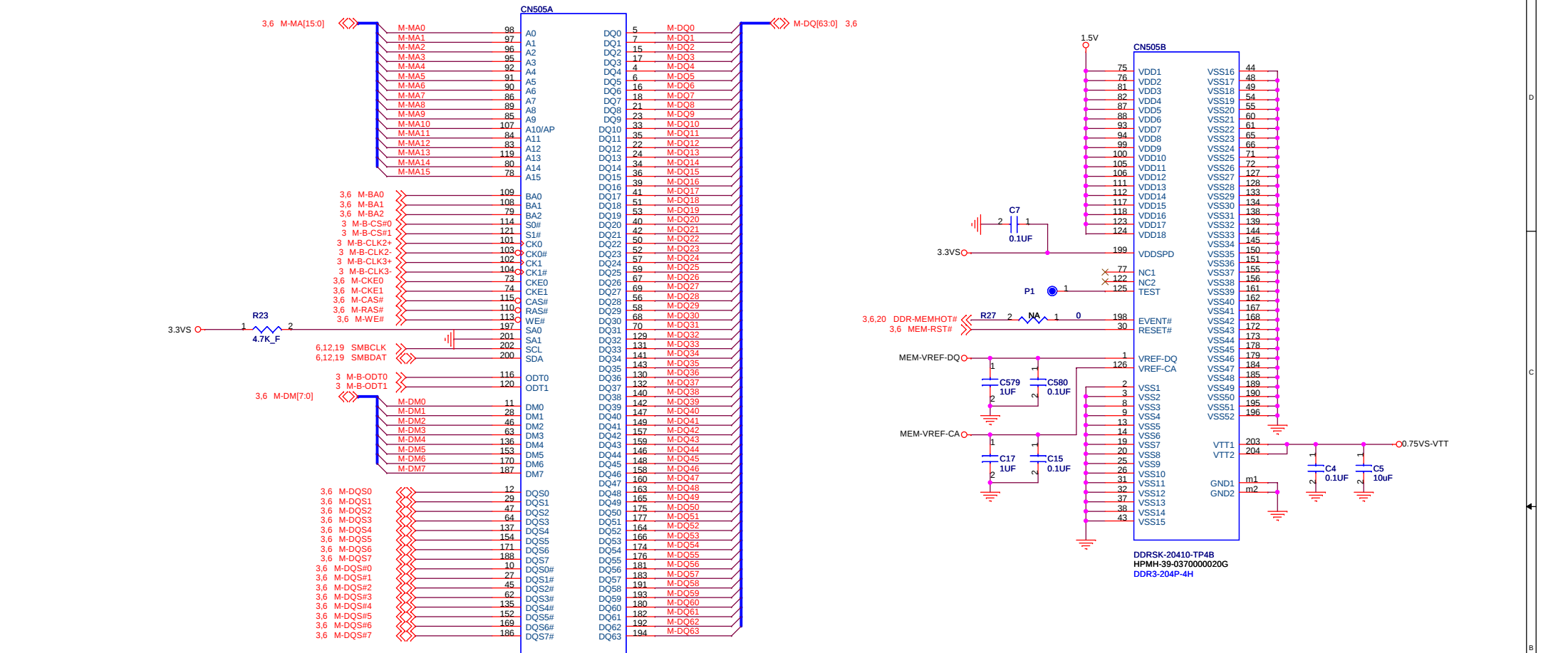
Layout :
Place near So-DimmA



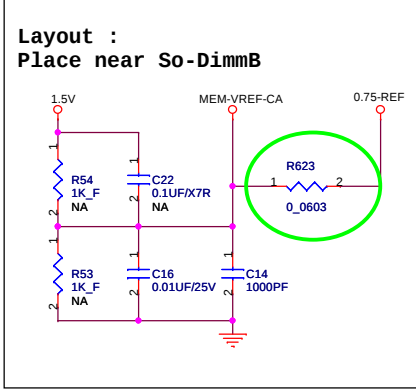
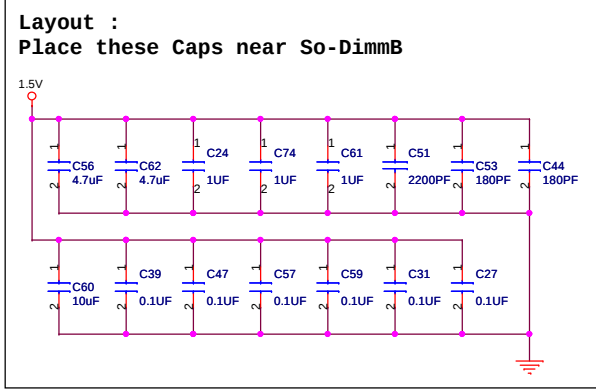
FLEX Computing

Project Name : H210UA1		Title : DDR3 SO-DIMM A	
Size :	Document Number :	HPMH-40GAB6000-C000	Rev : C
Date : Monday, September 27, 2010		Sheet : 6	of 28

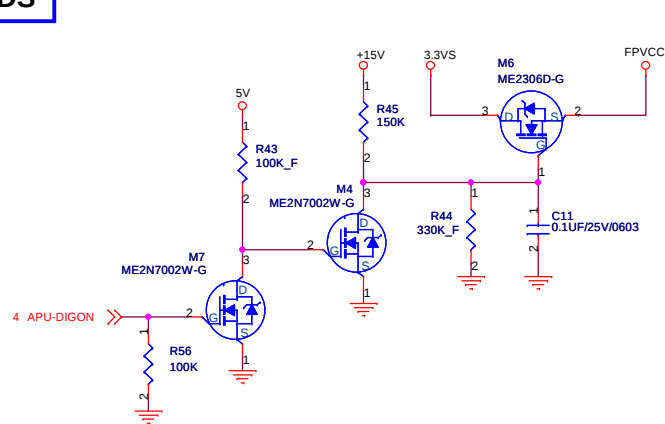
DDR3 DIMM B



SA0	SA1	Address
0	0	A0
1	0	A2

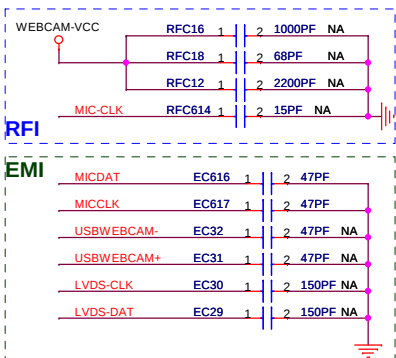
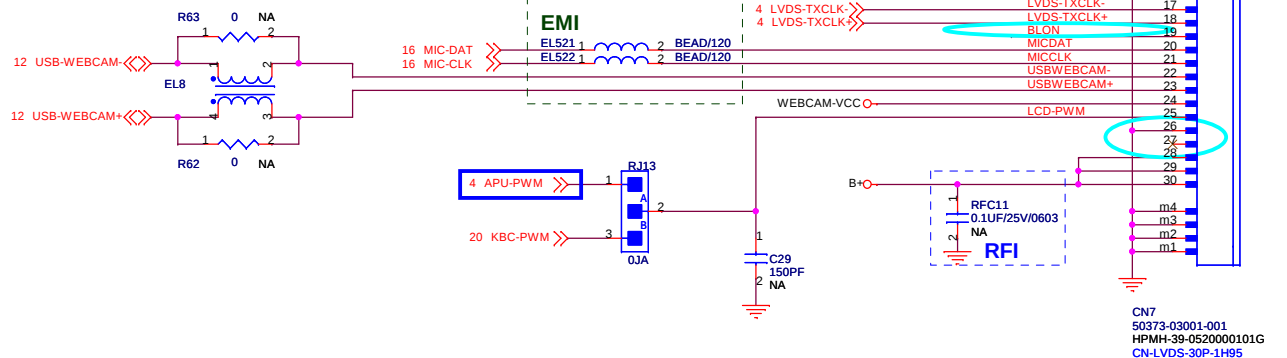


LVDS

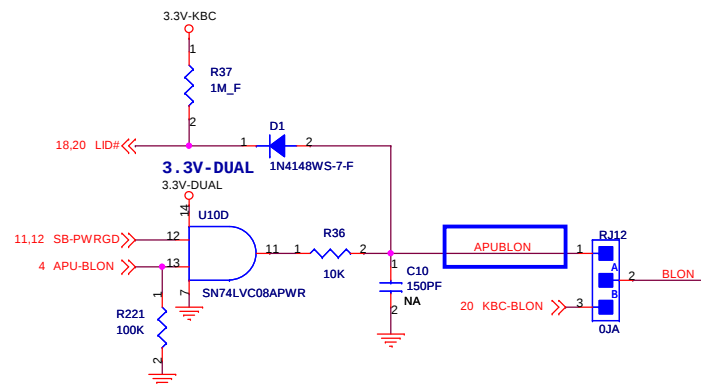
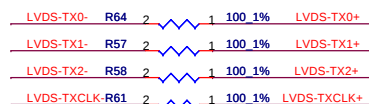


ME2306D-G VGS= 1(min) ~ 3(max)

+15= 11.8V ,VG=8.11V
VGS=8.11V-3.3V=4.81V
+15= 14.6V ,VG=10.03V
VGS=10.03V-3.3V=6.73V

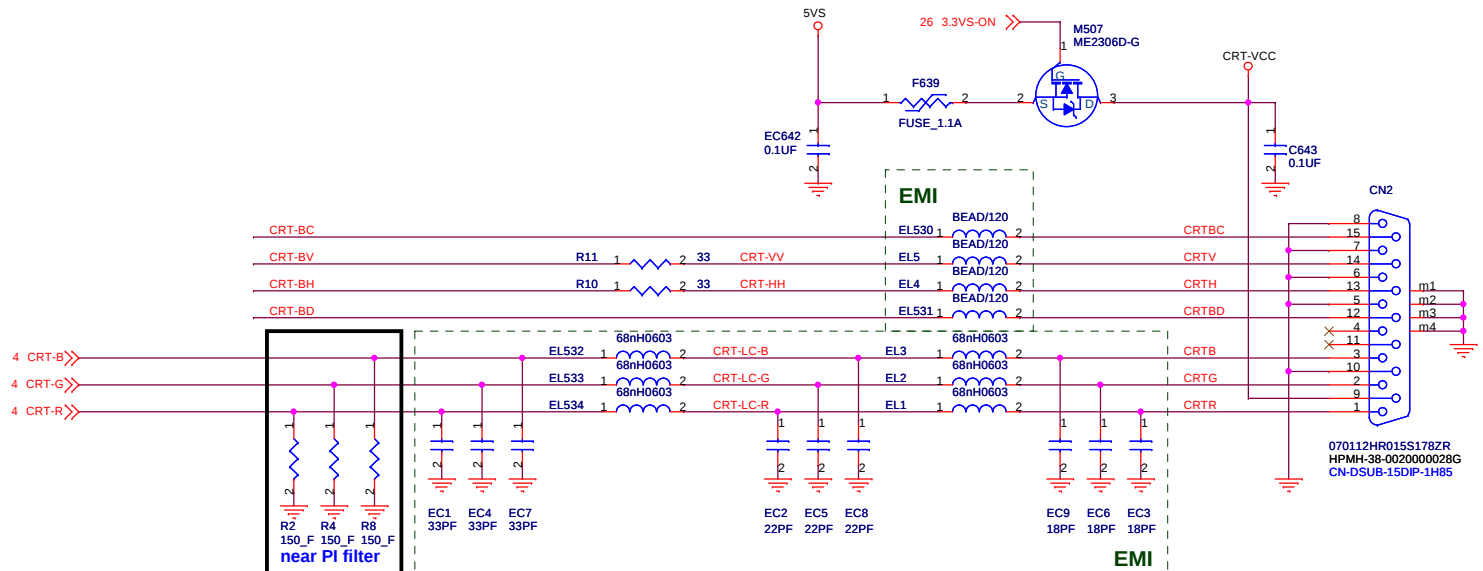


For DP to LVDS termination resistor

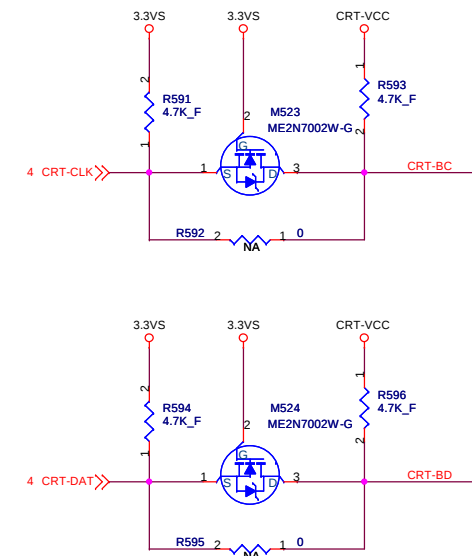


Mounted for AUO panel

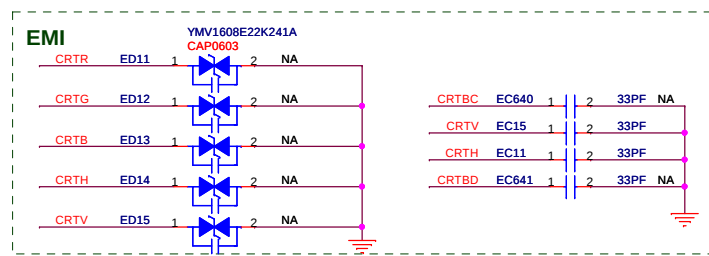
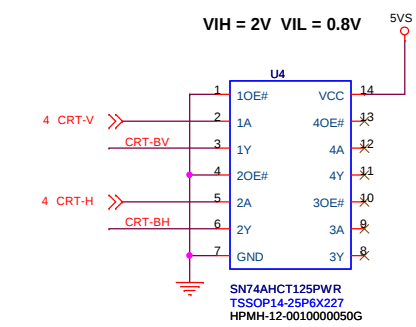
CRT



CRT LEVEL SHIFT



H / V SYNC BUFFER



INPUT		OUTPUT
nOE	nA	nY
L	L	L
L	H	H
H	X	Z

FLEXComputing

Project Name :

H210UA1

Title :

CRT Connector

Size :

Custom

Document Number :

HPMH-40GAB6000-C000

Rev :

C

Date :

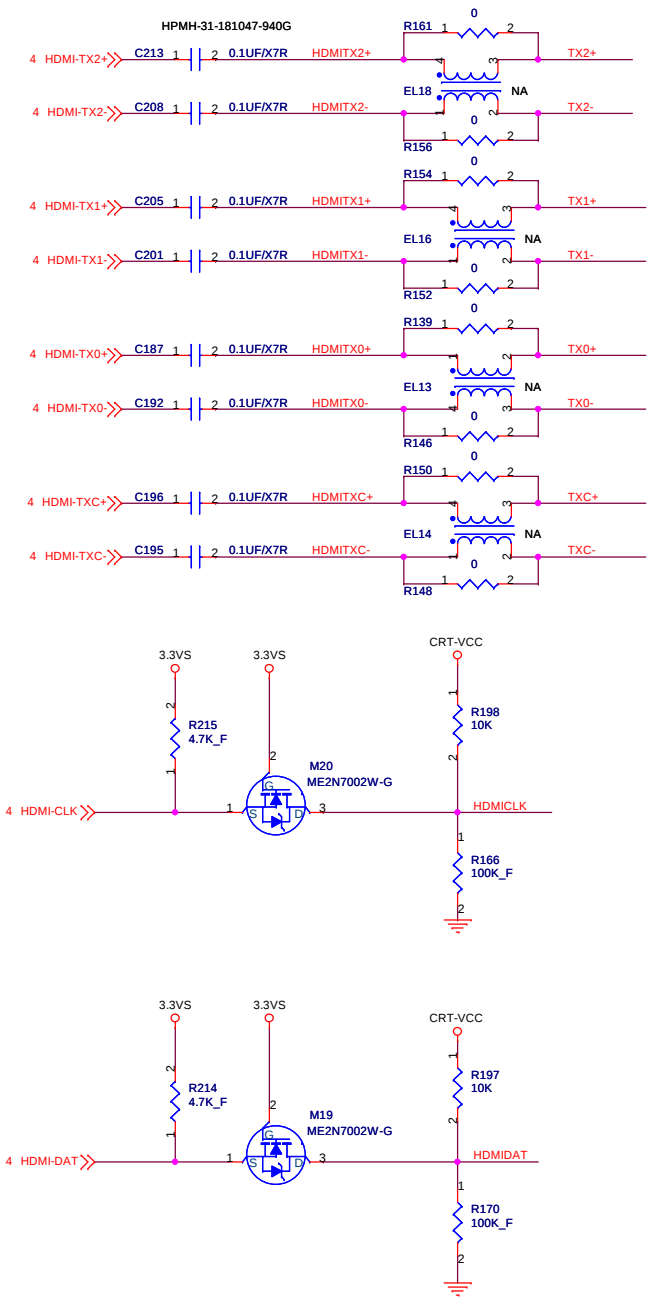
Monday, September 27, 2010

Sheet :

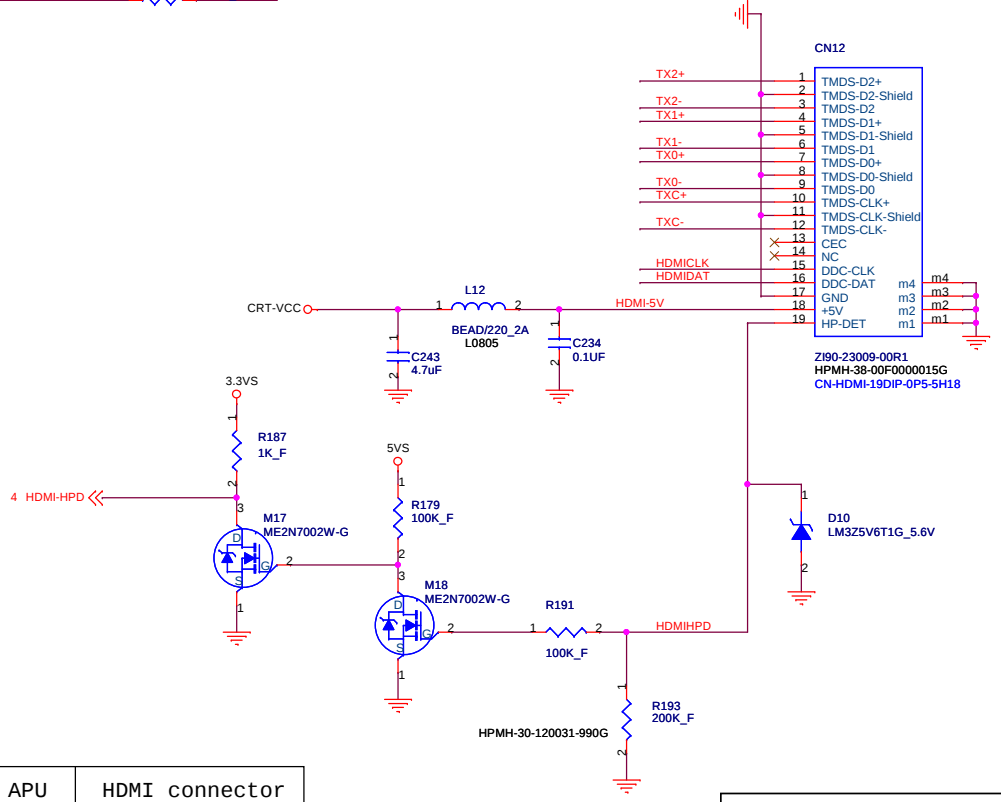
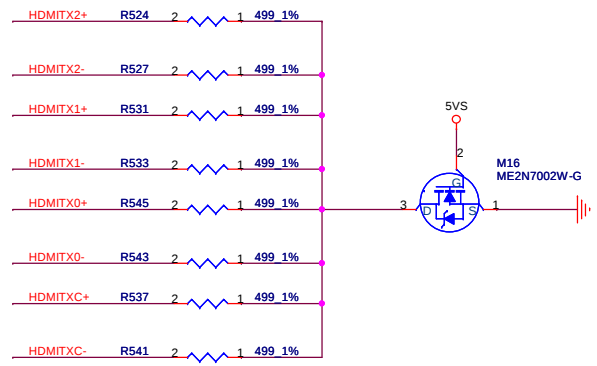
9 of 28

HDMI

CLOSE CN514

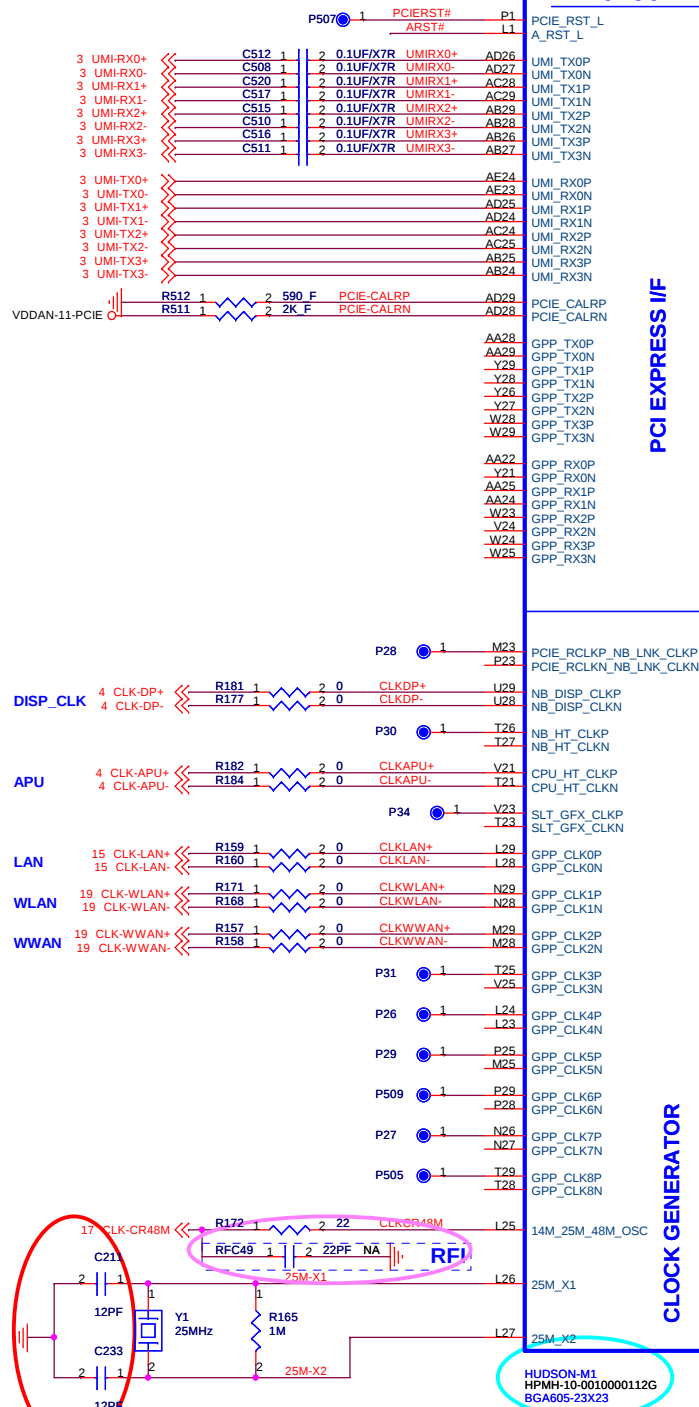


Connected a 499-Ω 5% resistor on each signal connected with a FET to GND (one FET per pair) located on the TMDS connector side of the series capacitors.



PLUG IN/OUT	APU	HDMI connector
IN	H	H
OUT	L	L

FCH_UMI/PCIE/CLK/LPC/RTC



HUDSON-1

PCI CLKs

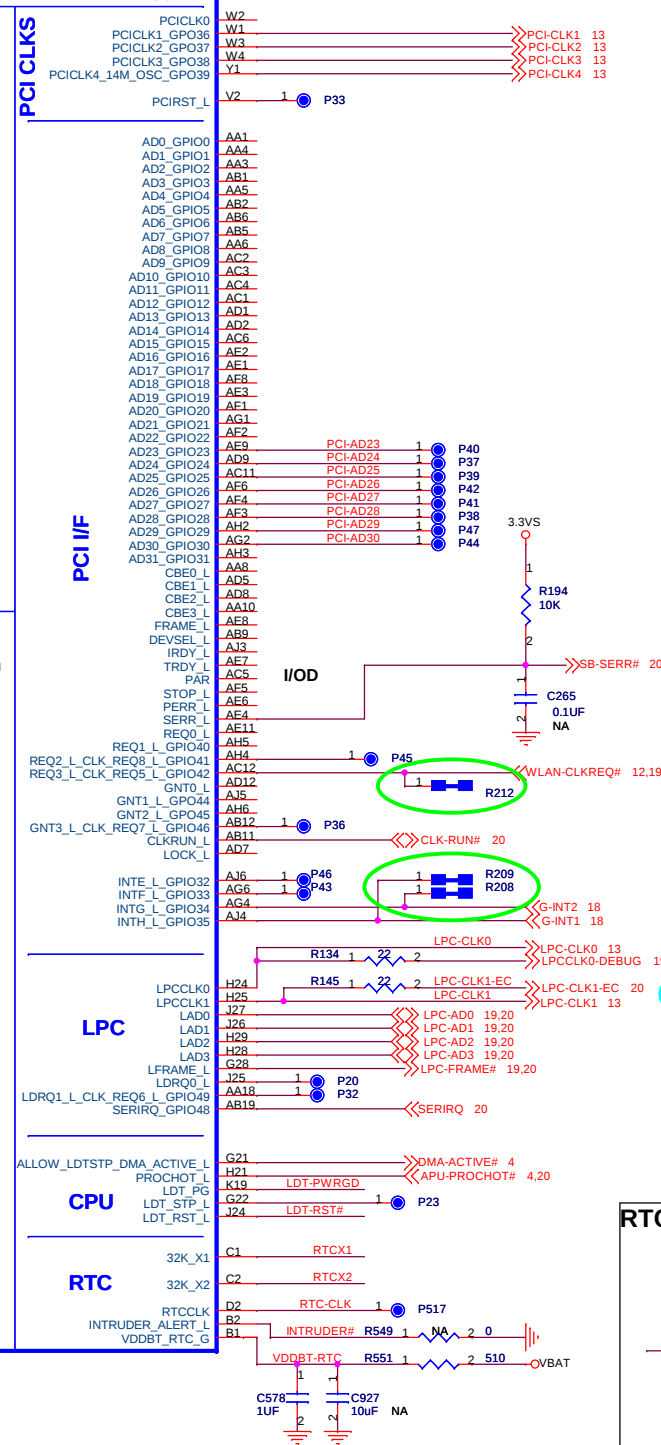
PCI EXPRESS I/F

PCI I/F

LPC

CPU

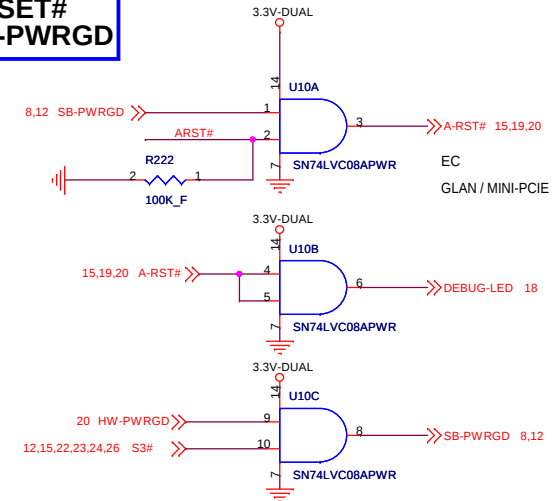
RTC



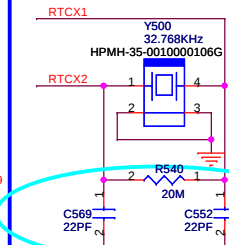
HUDSON-M1 DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

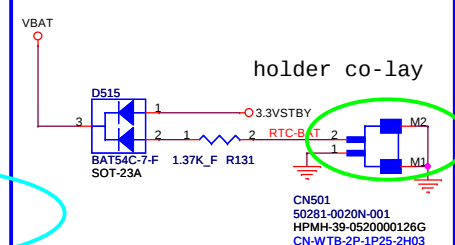
RESET#
SB-PWRGD



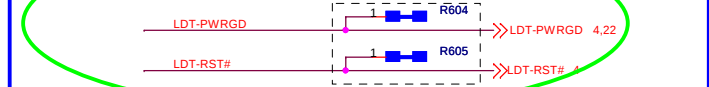
RTC CLOCK



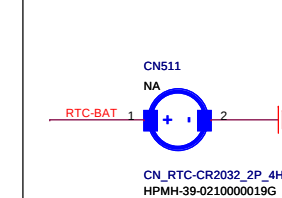
RTC BATTERY



Between U502 and U506



RTC Holder



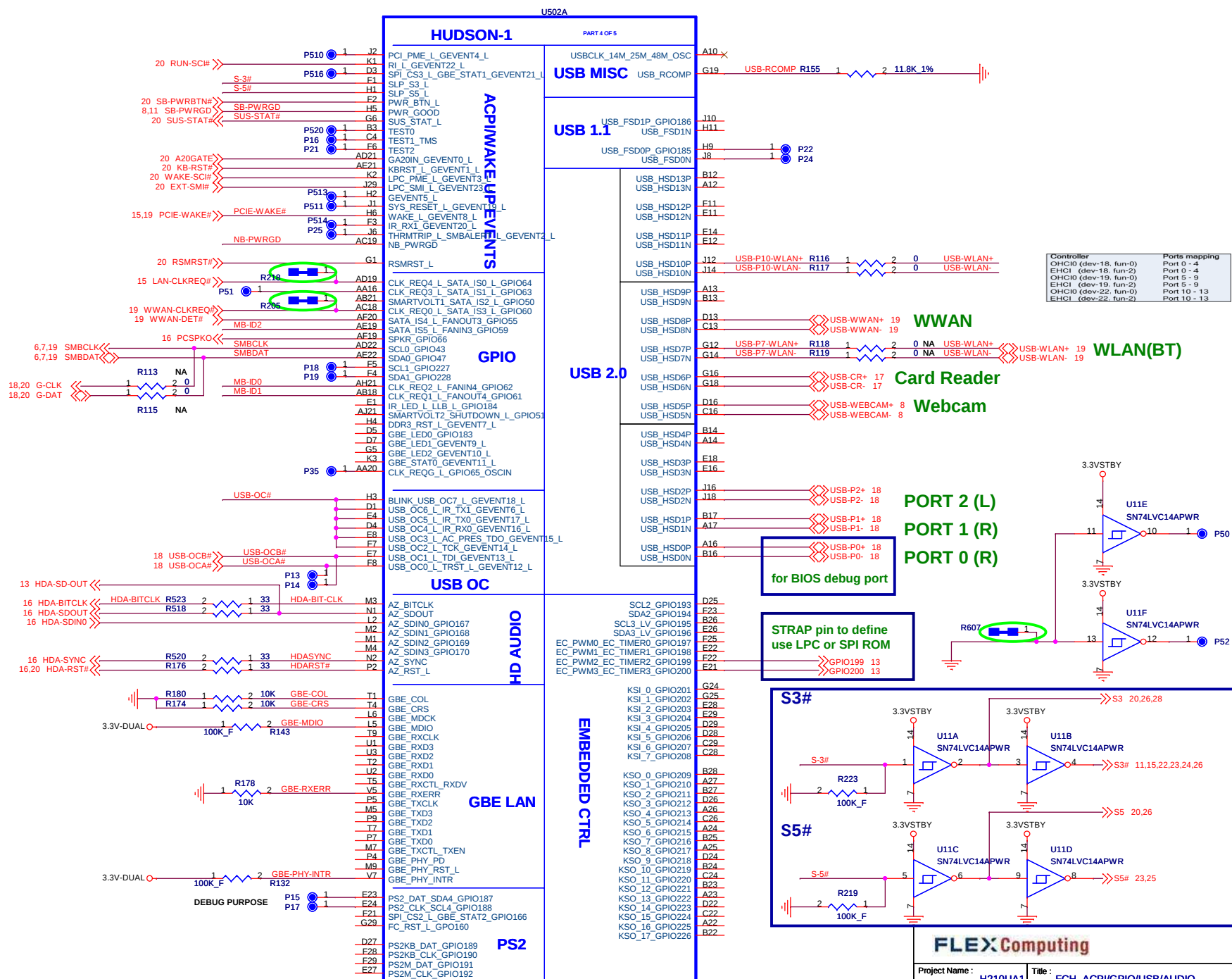
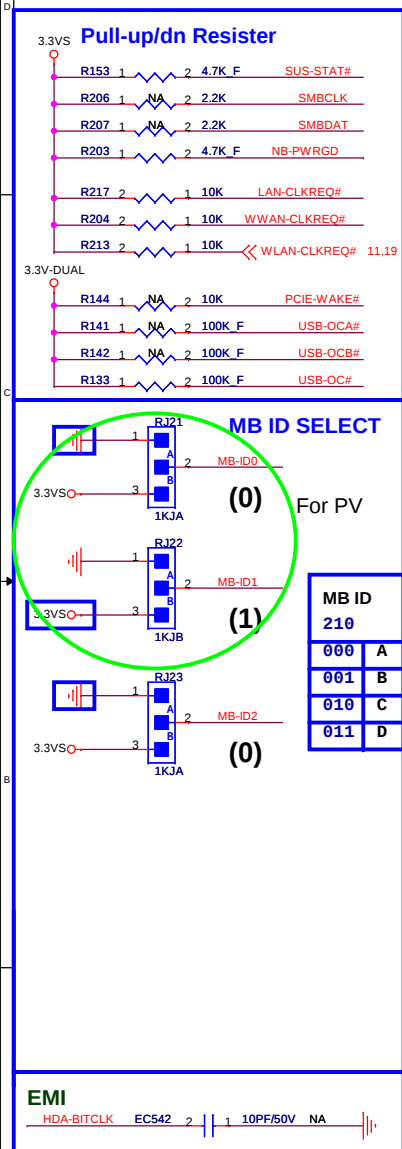
LPCCLK0-DEBUG		RFC639	1	2	22PF	NA
LPC-CLK1-EC		RFC640	1	2	22PF	NA

RFI

FLEX Computing

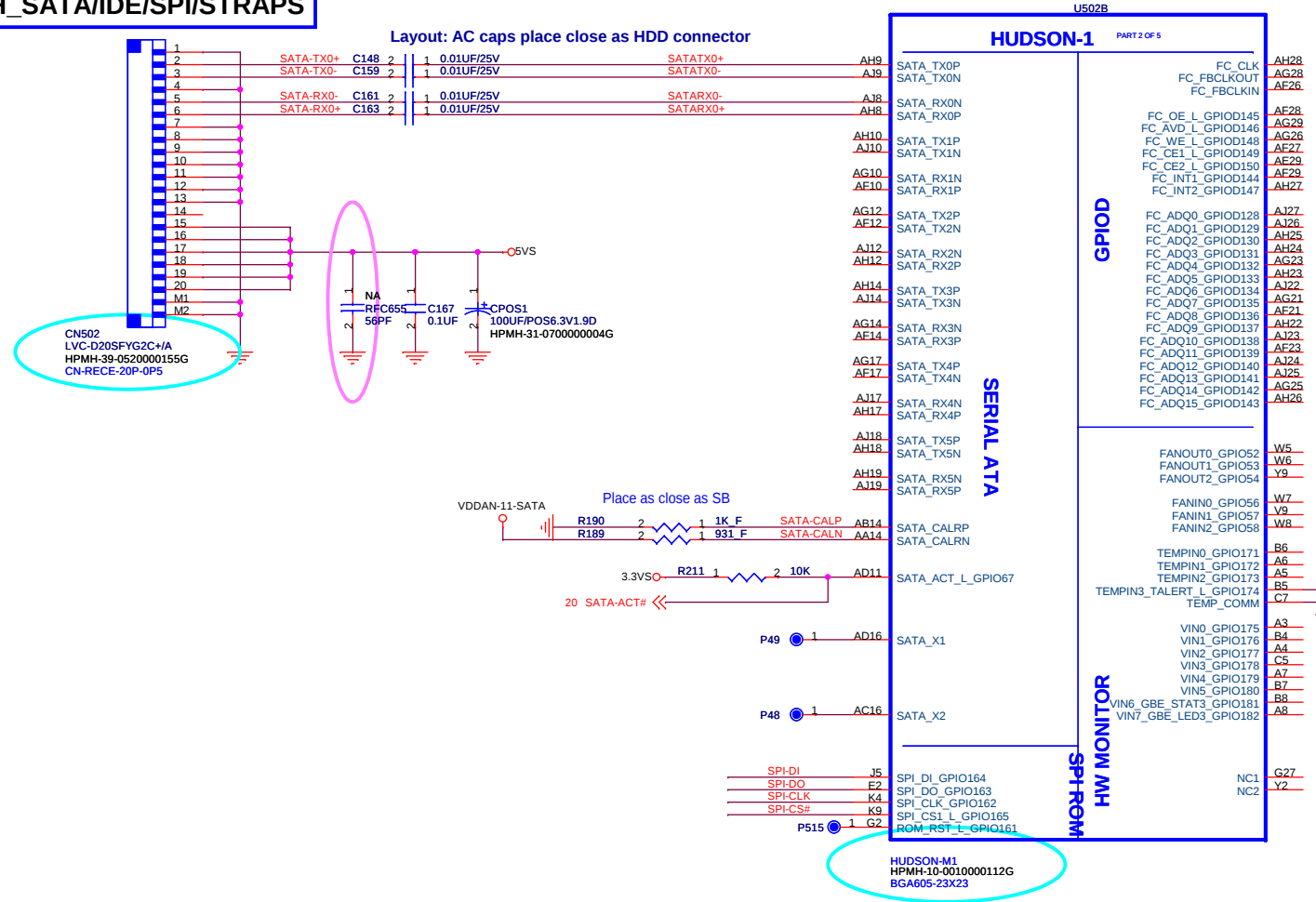
Project Name :		H210UA1		Title :	FCH_UM/PCIE/CLK/LPC/RTC	
Size :	Document Number :				HPMH-40GAB6000-C000	Rev : C
Date: Monday, October 04, 2010				Sheet : 11 of 28		

FCH_ACPI/GPIO/USB/AUDIO

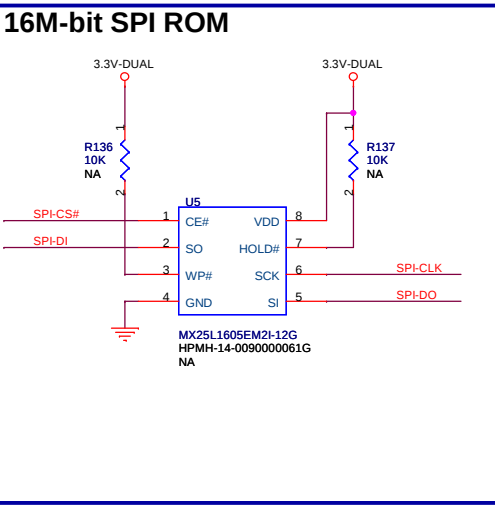


HUDSON-M1
HPMH-10-0010000112G
BGA605-23X23

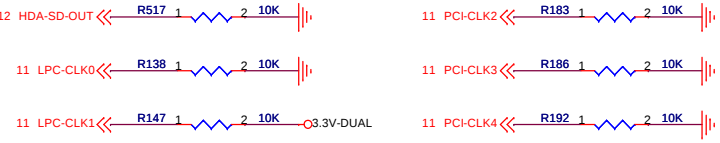
FCH_SATA/IDE/SPI/STRAPS



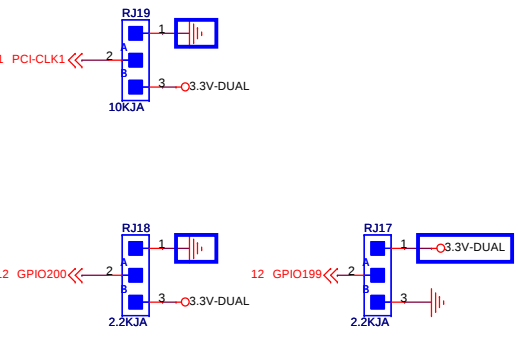
SATA / IDE / SPI / STRAPS



HUDSON-M1 HW STRAPS



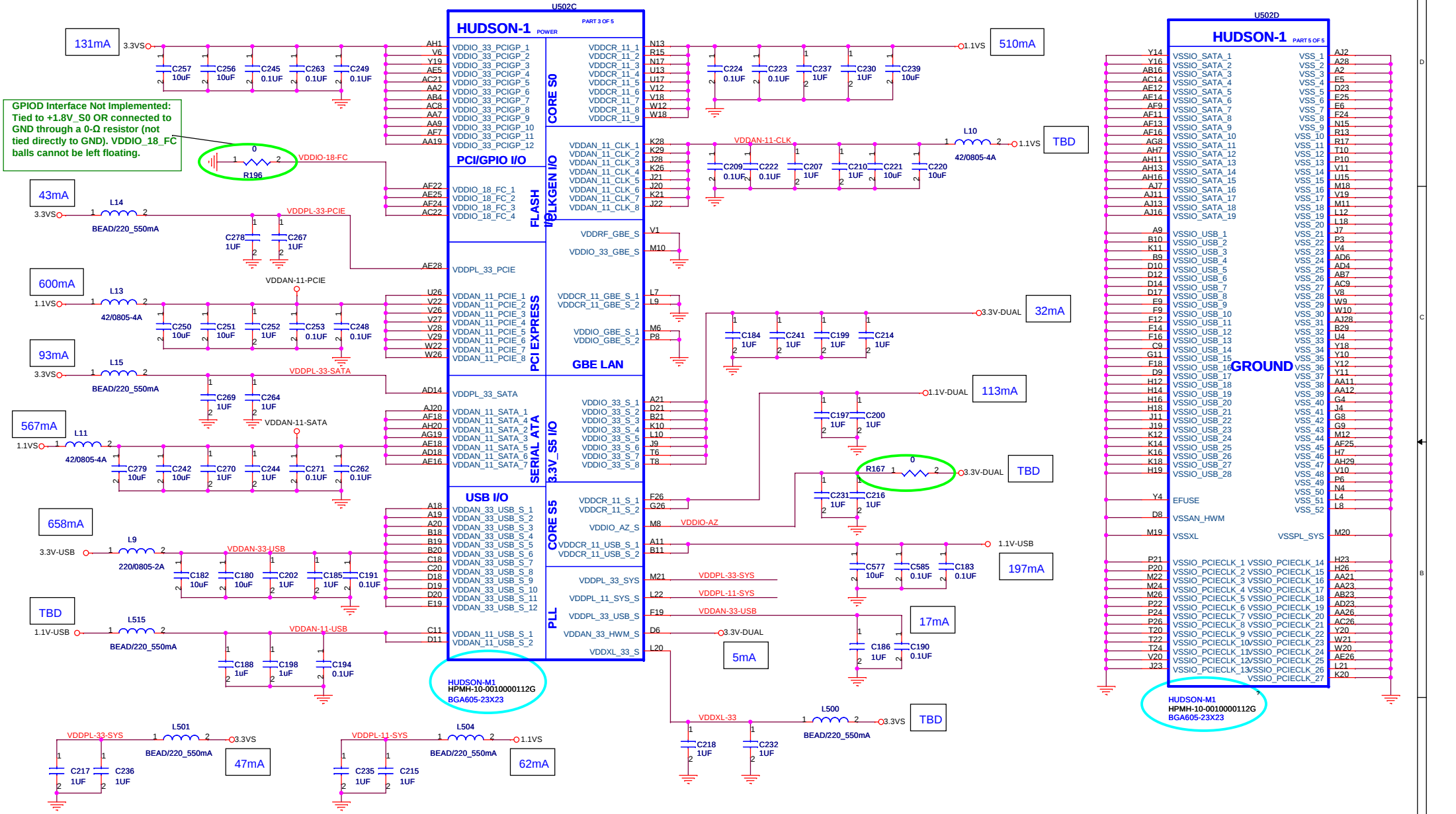
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	



FLEX Computing

Project Name :	H210UA1	Title :	FCH_SATA/IDE/SPI/STRAPS
Size :	Document Number :	HPMH-40GAB6000-C000	Rev : C
Date :	Monday, September 27, 2010	Sheet :	13 of 28

GPIO Interface Not Implemented:
Tied to +1.8V_S0 OR connected to
GND through a 0-Ω resistor (not
tied directly to GND). VDDIO_18_FC
balls cannot be left floating.



3.3V-USB / 1.1V-USB	S3	S4	S5
AC mode	ON	OFF	OFF
DC mode	OFF	OFF	OFF

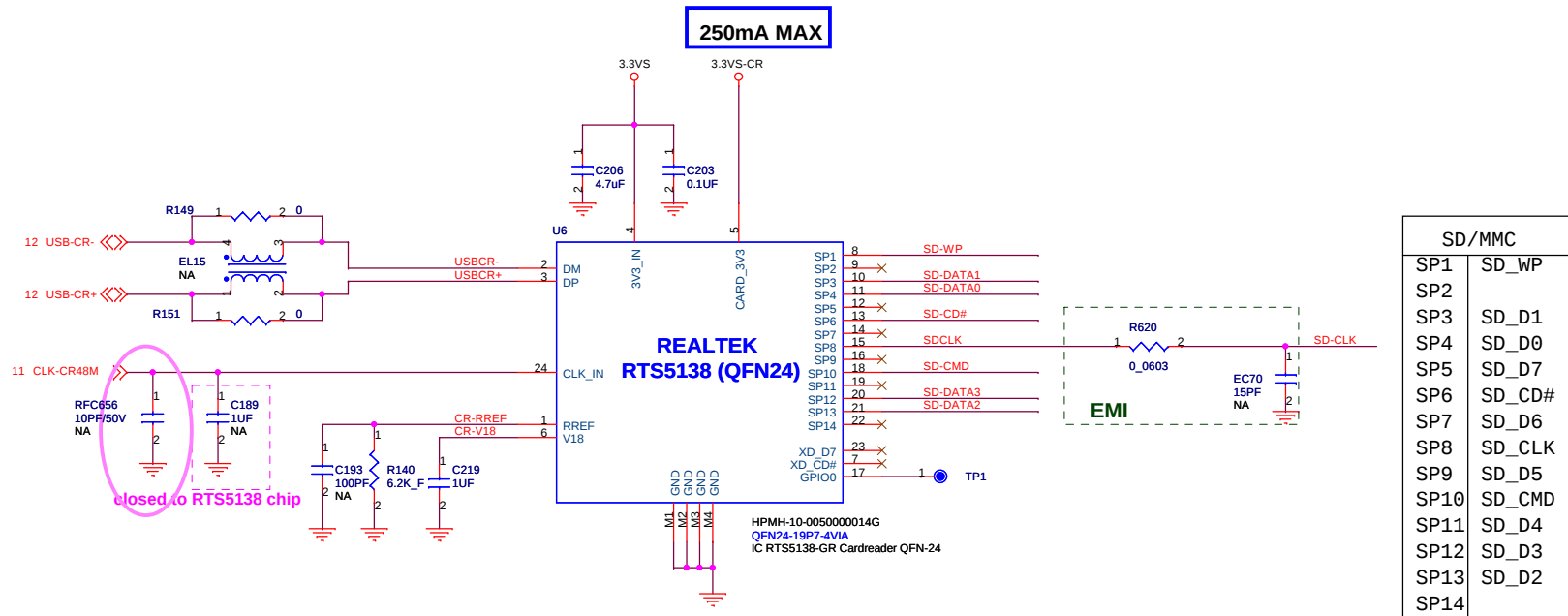
FLEXComputing

Project Name : H210UA1Title : FCH_PWR/GND

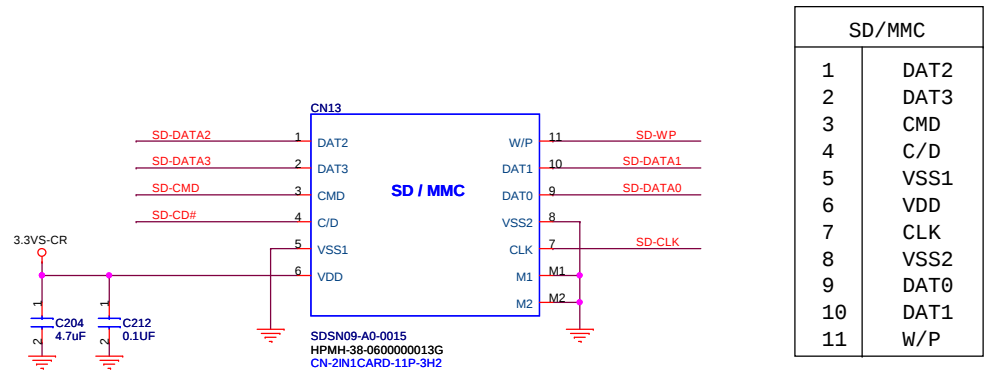
Size : Document Number : HPMH-40GAB6000-C000Rev : c

Date : Thursday, September 23, 2010Sheet : 14 of 28

Card Reader

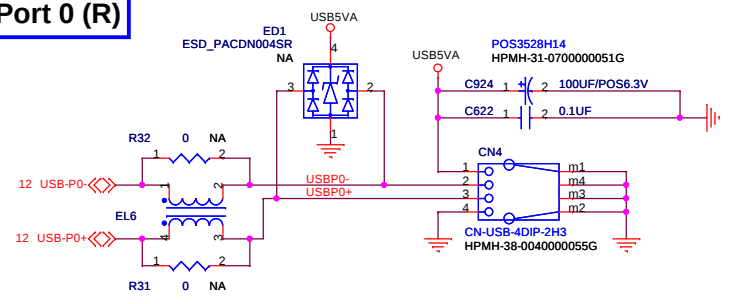


Memory Card Socket

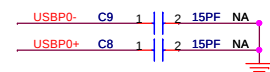


SD/MMC	
1	DAT2
2	DAT3
3	CMD
4	C/D
5	VSS1
6	VDD
7	CLK
8	VSS2
9	DAT0
10	DAT1
11	W/P

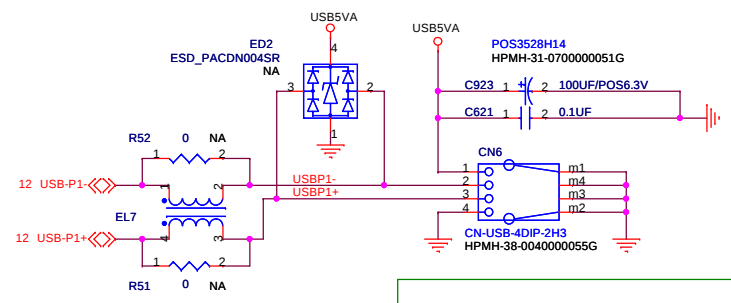
USB Port 0 (R)



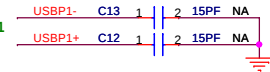
Note 1
For USB ports that have trace length of <=10", the rise and fall time parameters may not meet the specification of > 450 ps.



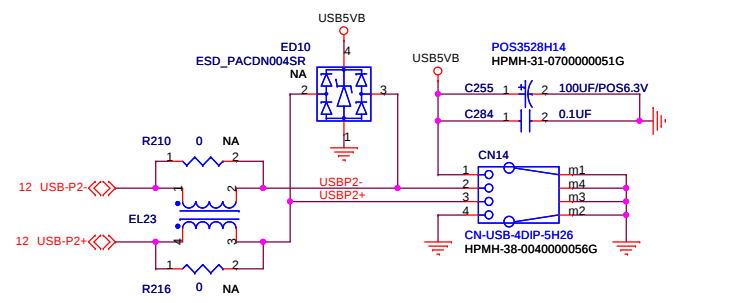
USB Port 1 (R)



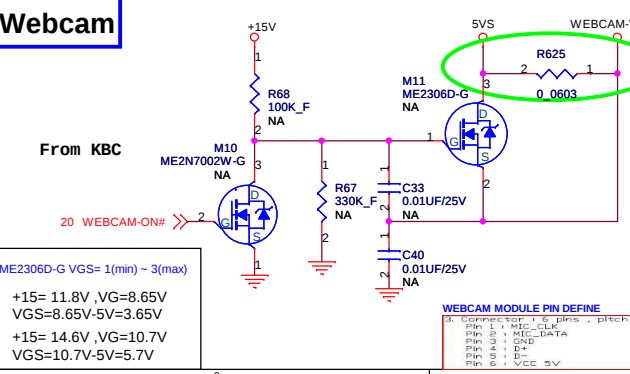
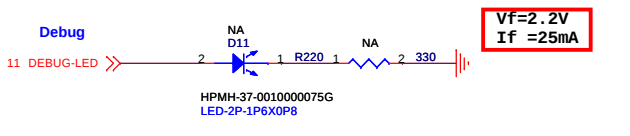
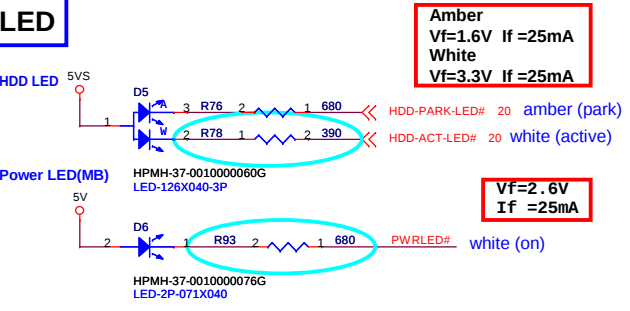
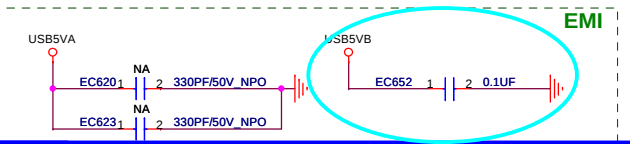
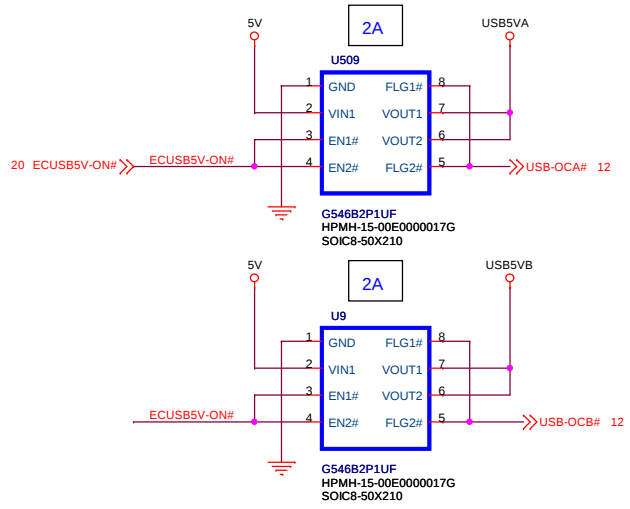
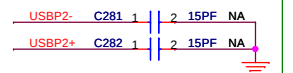
Note 1
For USB ports that have trace length of <=10", the rise and fall time parameters may not meet the specification of > 450 ps.



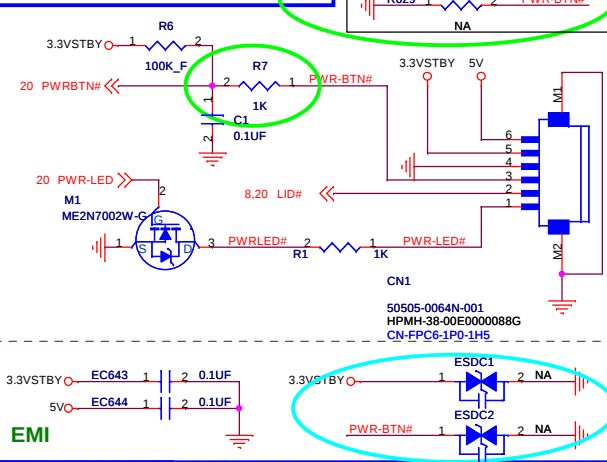
USB Port 2 (L)



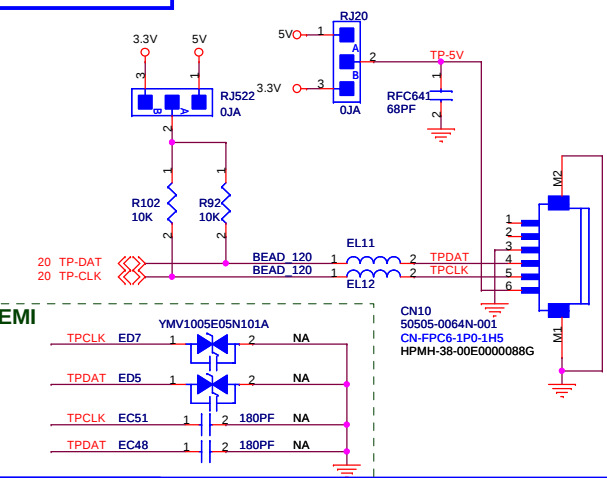
Note 1
For USB ports that have trace length of <=10", the rise and fall time parameters may not meet the specification of > 450 ps.



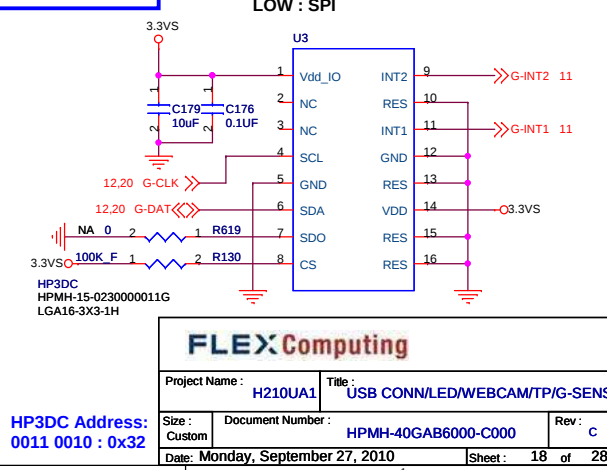
Power Button DB CONN



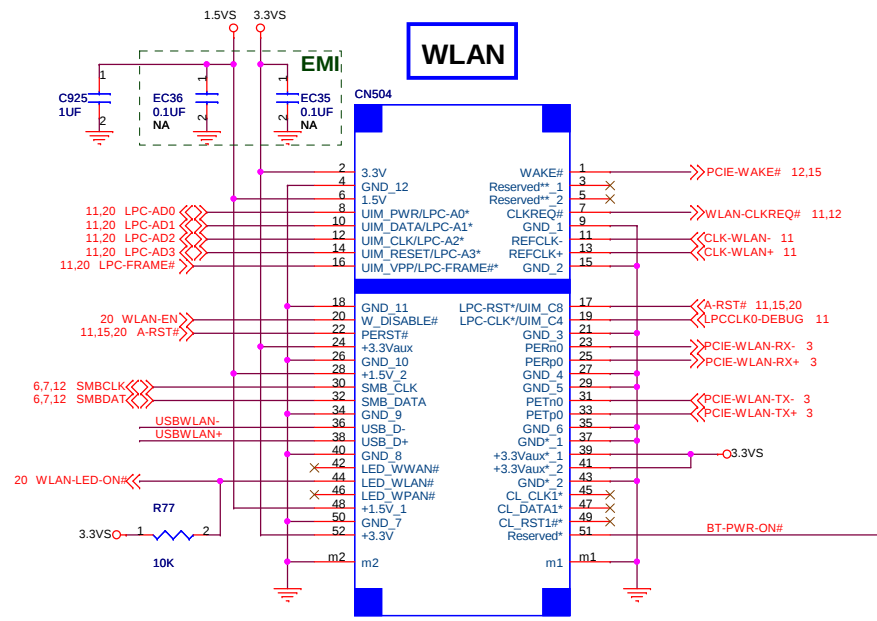
Touch Pad



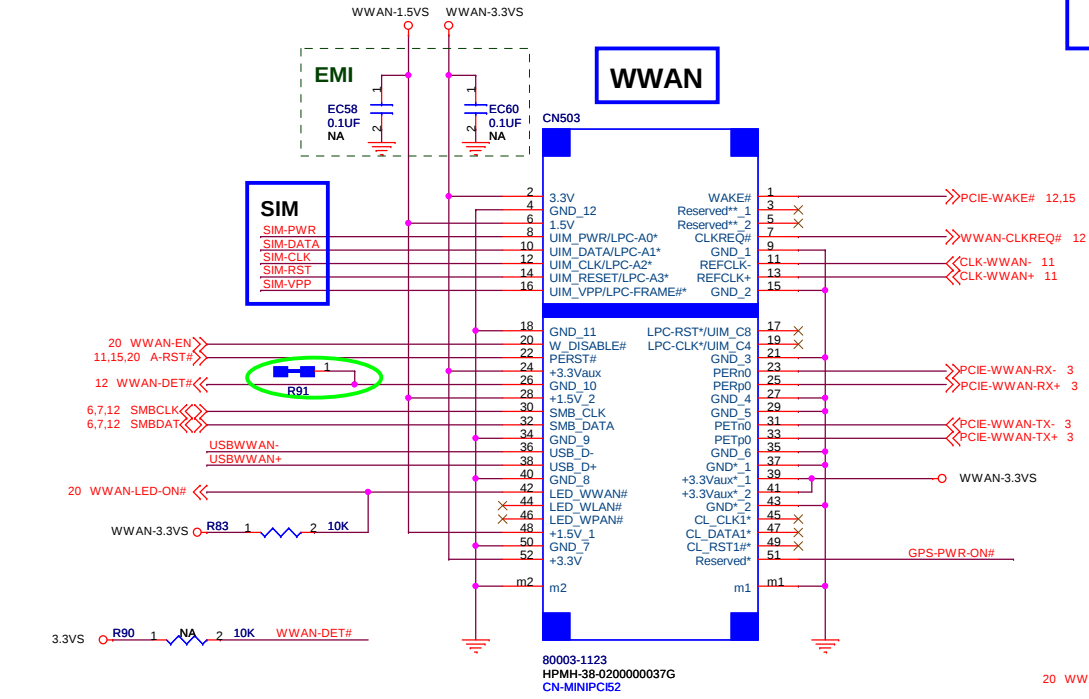
G-Sensor



WLAN / WWAN

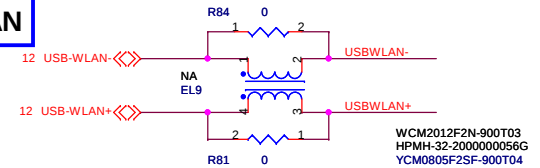


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HPMH-38-0200000037G
CN-MINIPC52

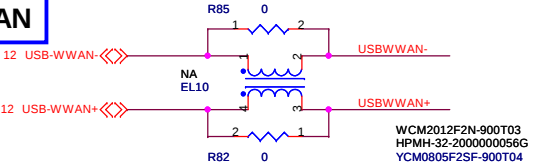


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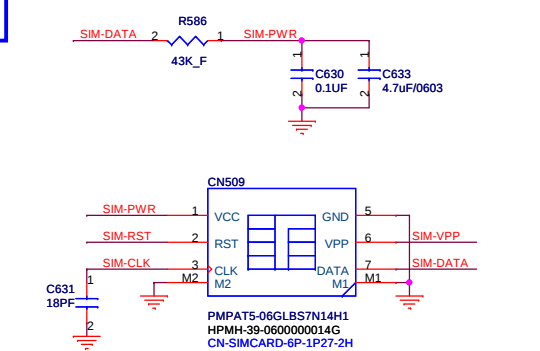
WLAN



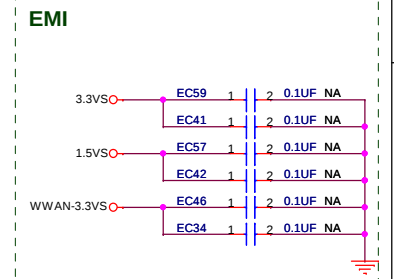
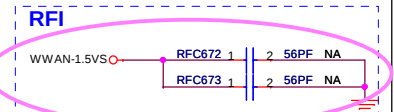
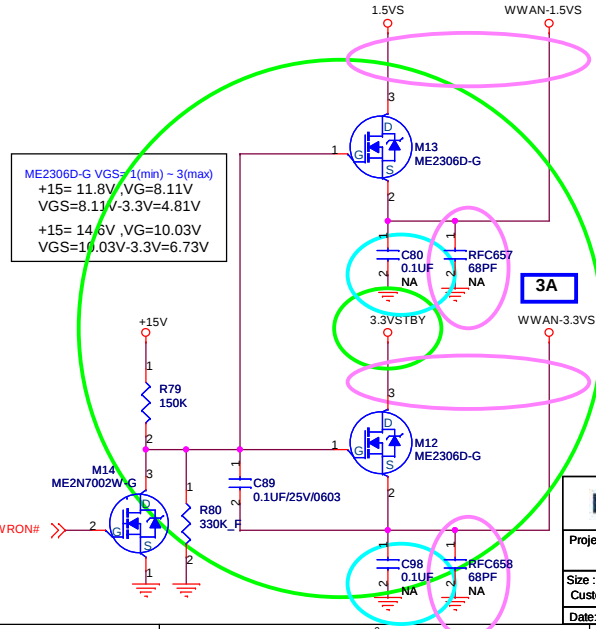
WWAN



SIM

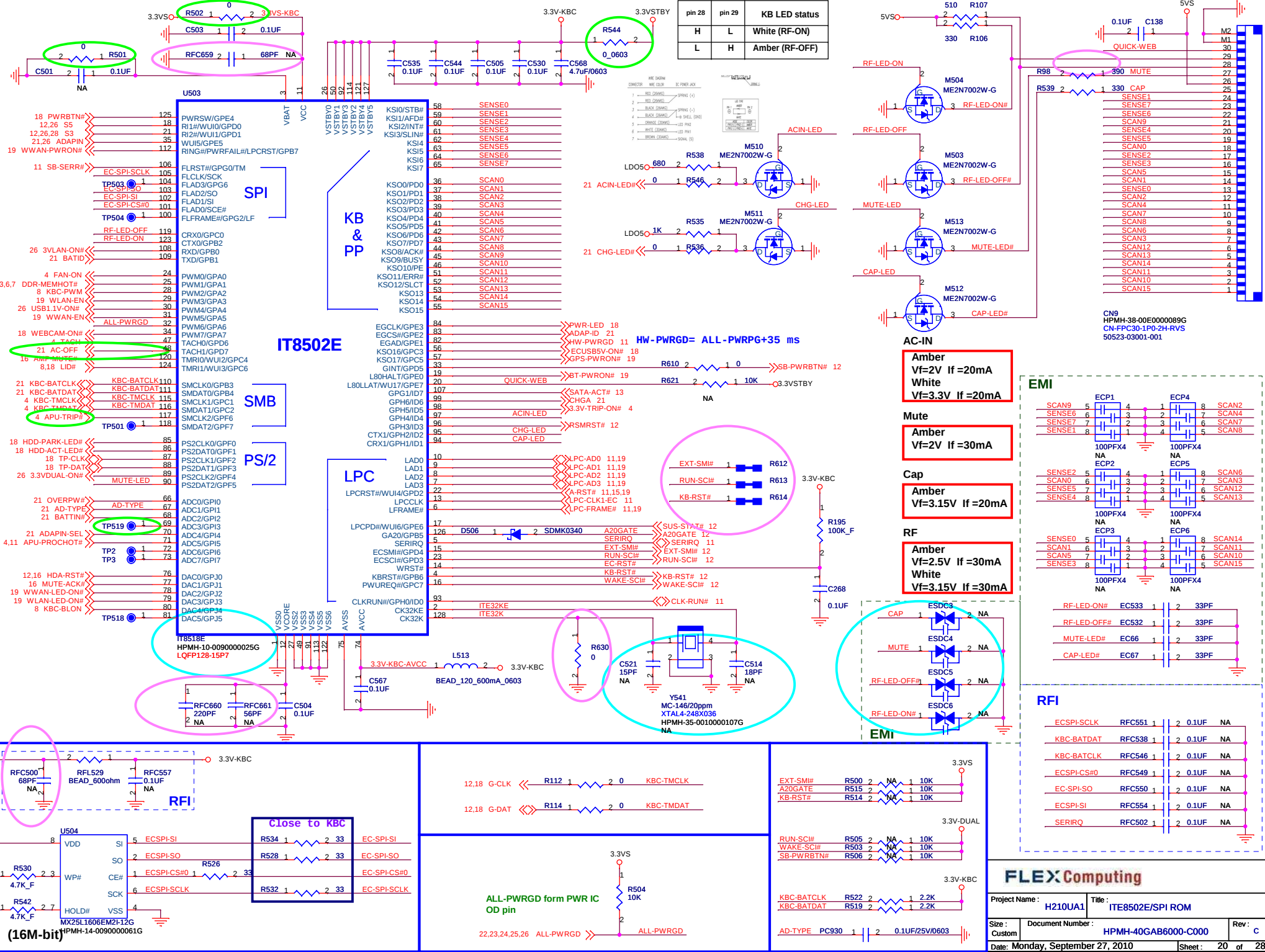


0.5A

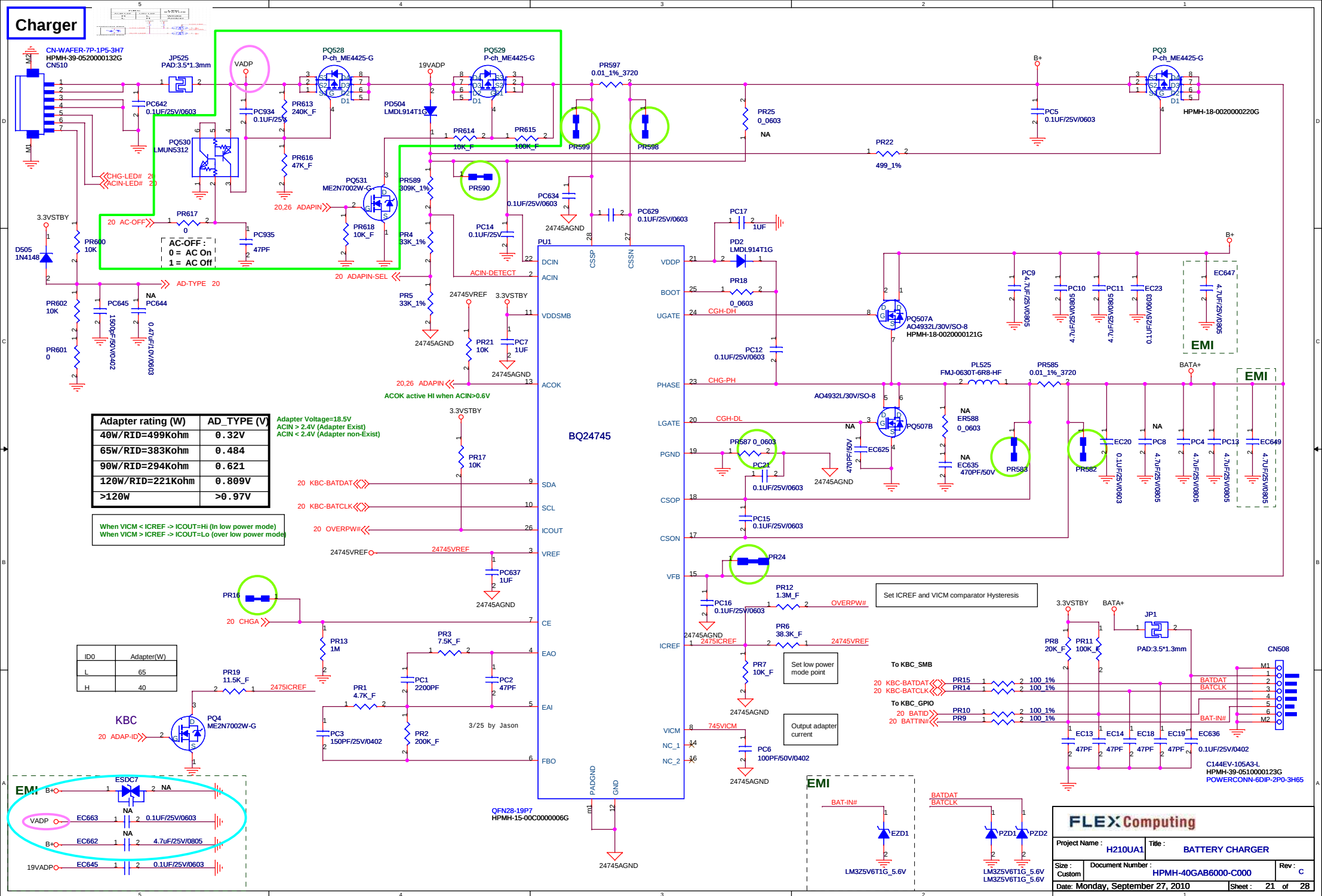


FLEX Computing

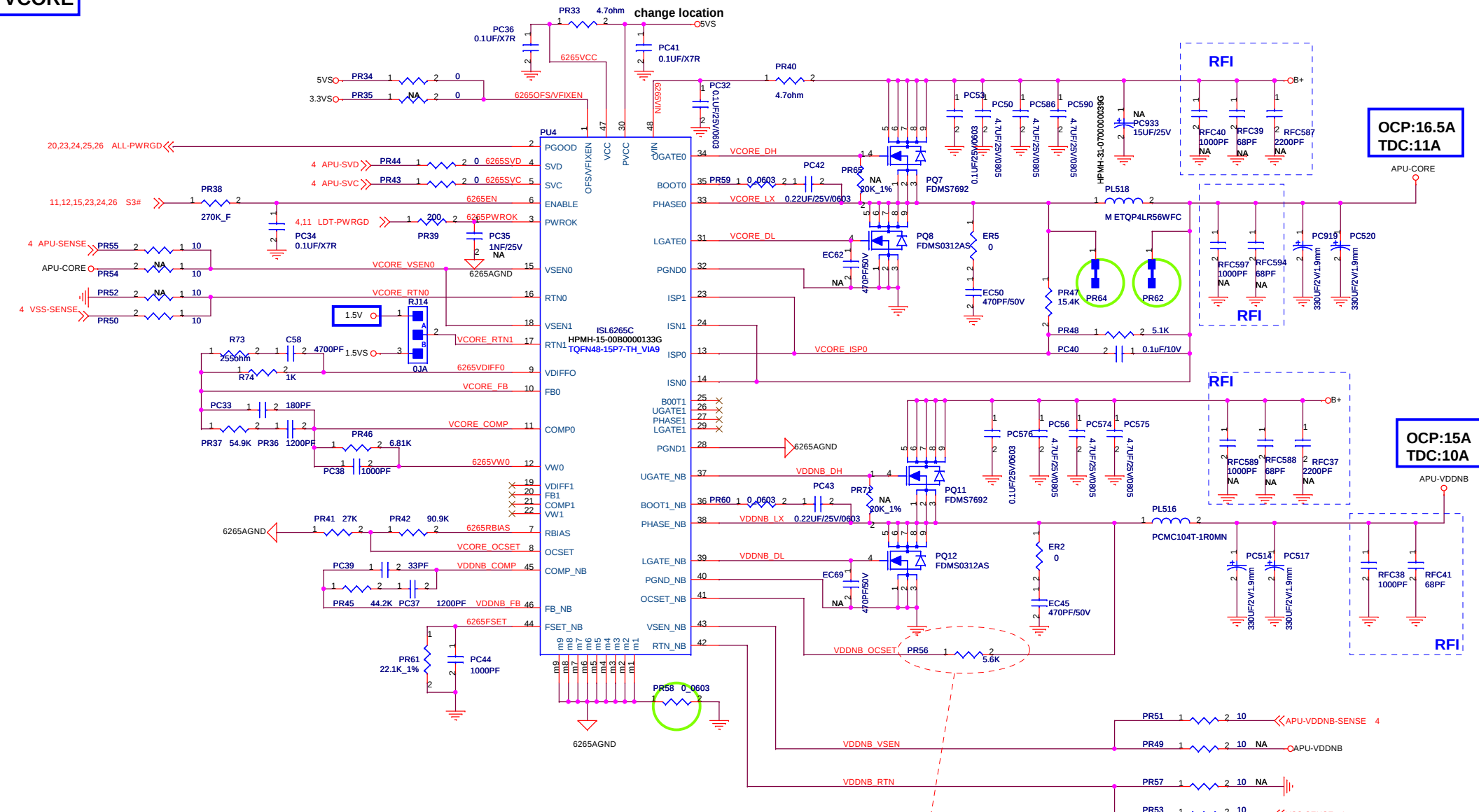
Project Name :	H210UA1	Title :	WLAN/WWAN/BT/SIM
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Charger



VCORE

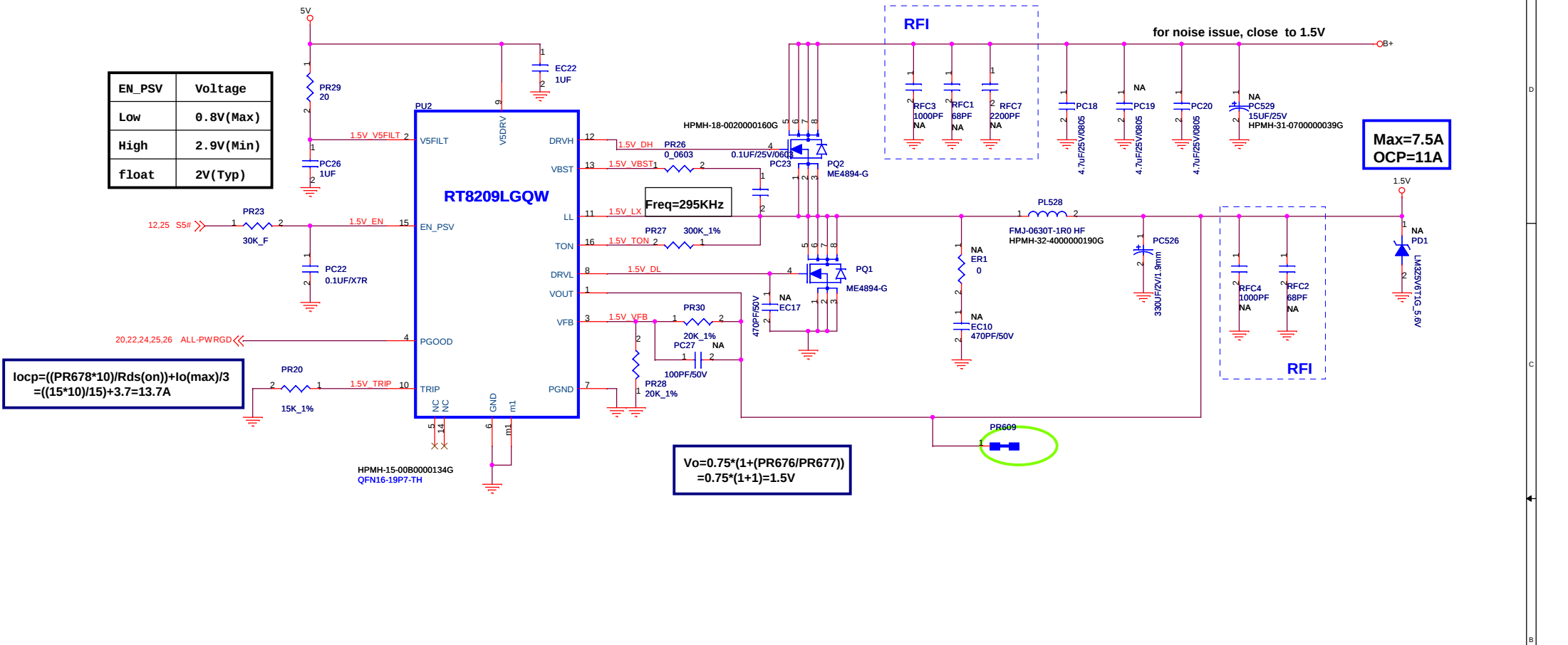

$$\text{RocsetNB} = \text{Ioc} * \text{Rdson} / 10\mu\text{A}$$

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

1.5VDDR



0.75VS

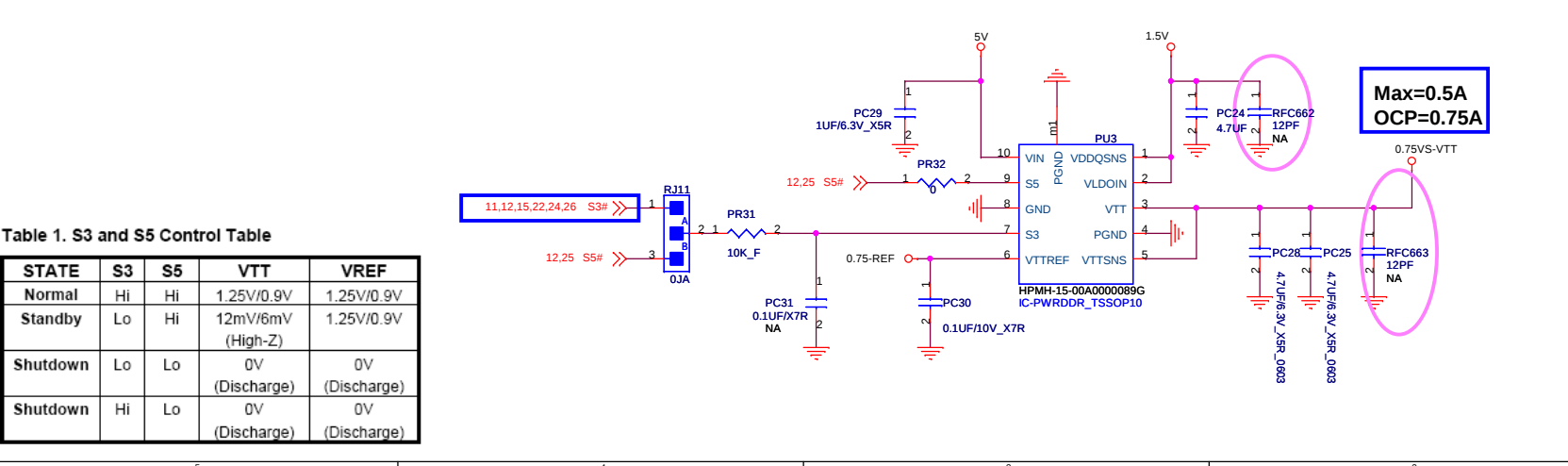
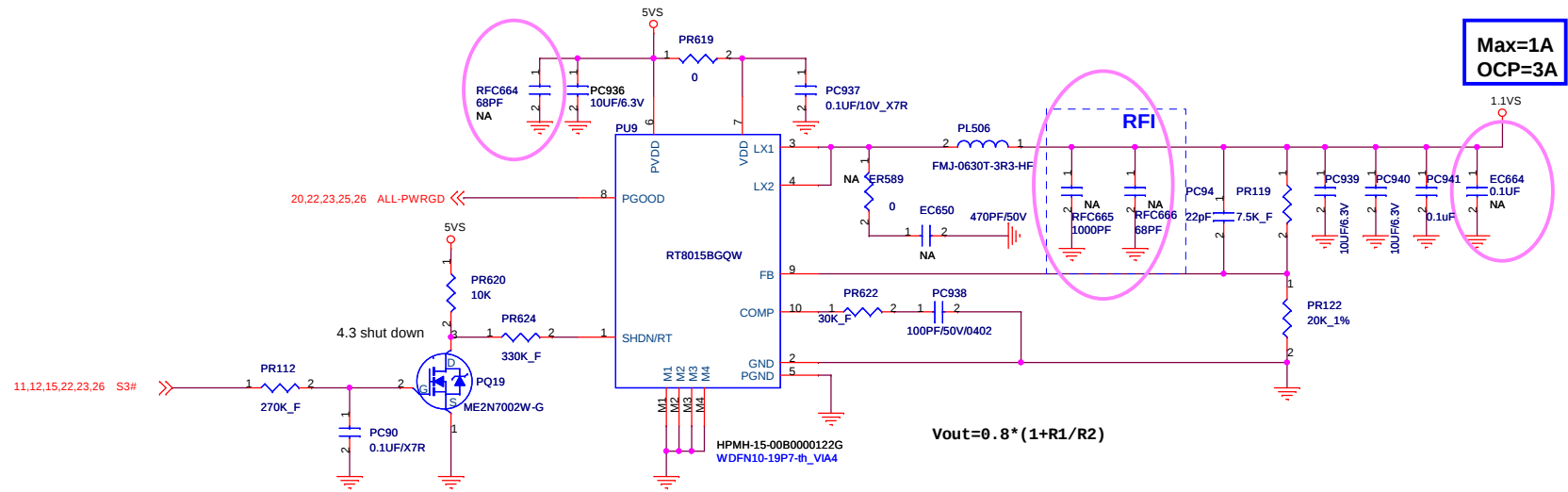


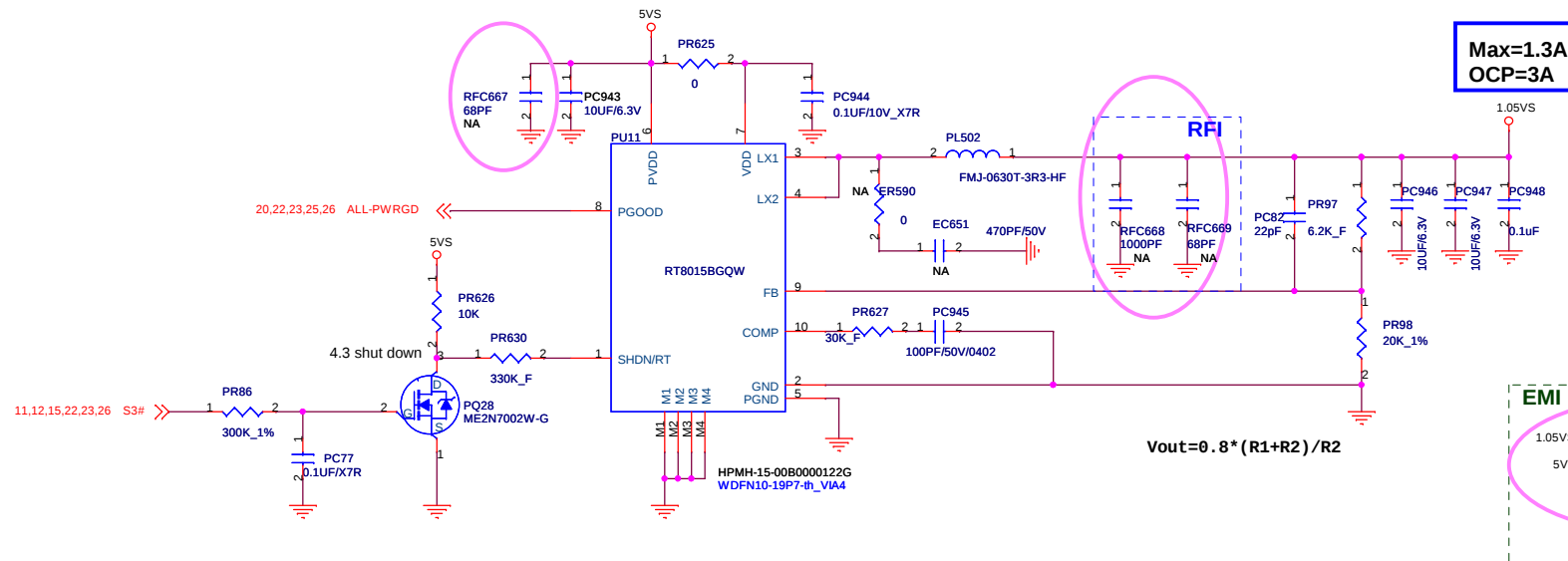
Table 1. S3 and S5 Control Table

STATE	S3	S5	VTT	VREF
Normal	Hi	Hi	1.25V/0.9V	1.25V/0.9V
Standby	Lo	Hi	12mV/6mV (High-Z)	1.25V/0.9V
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)
Shutdown	Hi	Lo	0V (Discharge)	0V (Discharge)

1.1VS



1.05VS



S4/S3 OFF

5VS

Control HDMI CONN 5V

3.3VS

1.5VS

3.3V

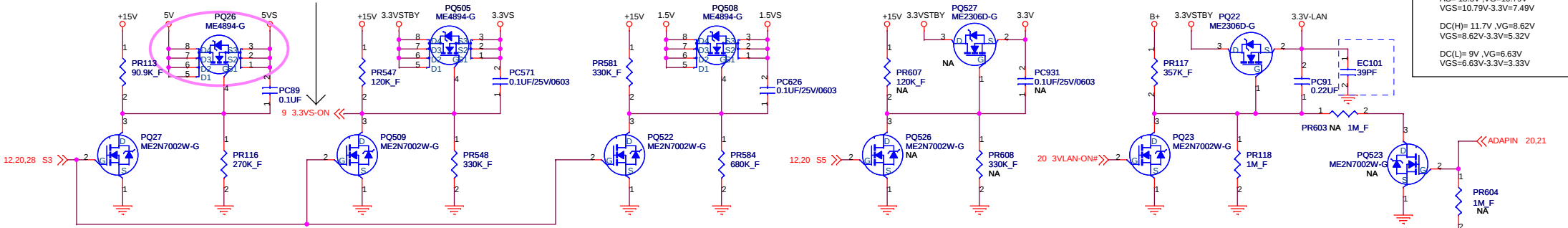
3.3V-LAN

rise time 1 ~100ms

AC= 18.5V ,VG=10.79V
VGS=10.79V-3.3V=7.49V

DC(H)= 11.7V ,VG=8.62V
VGS=8.62V-3.3V=5.32V

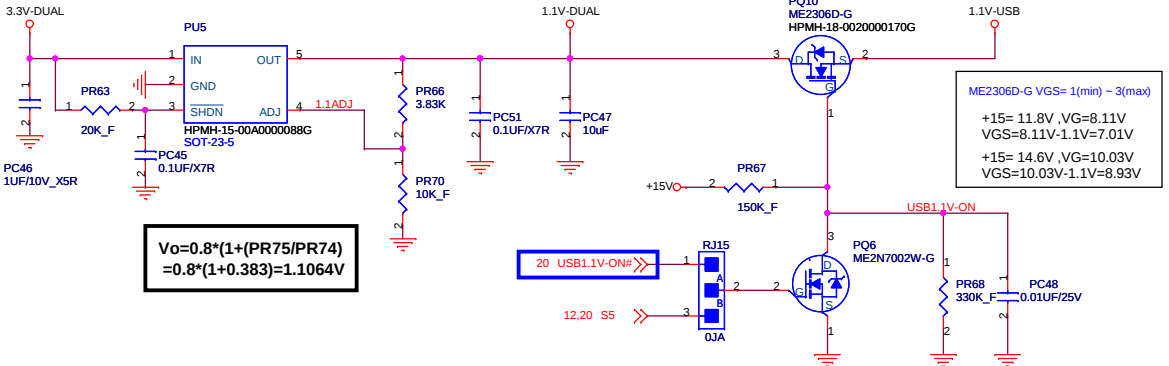
DC(L)= 9V ,VG=6.63V
VGS=6.63V-3.3V=3.33V



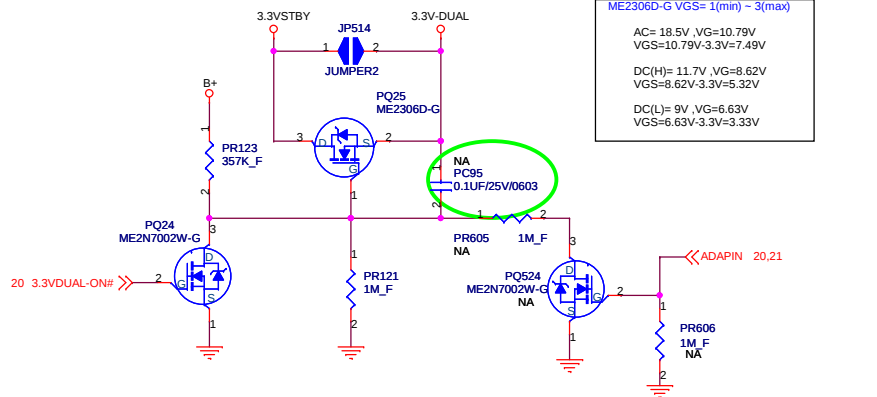
1.1VSTBY / 1.1V_USB

200mA

150mA



3.3V-DUAL



1.8VS

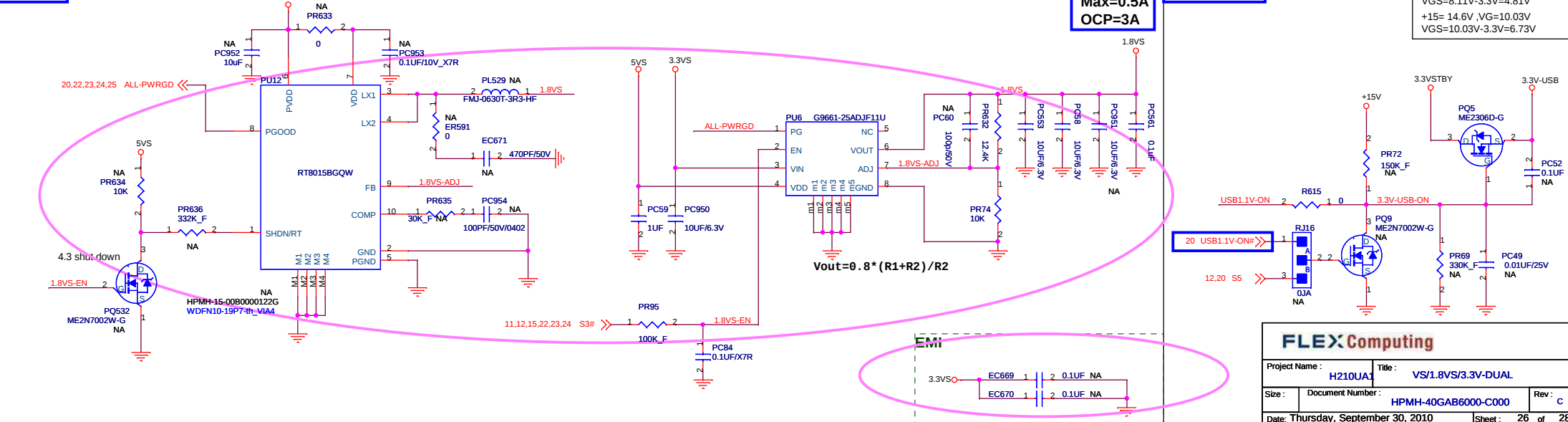
Max=0.5A OCP=3A

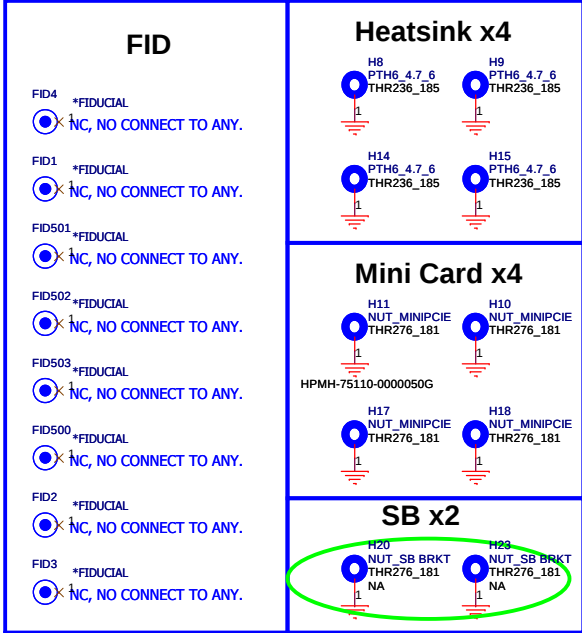
3.3V-USB

ME2306D-G VGS= 1(min) ~ 3(max)

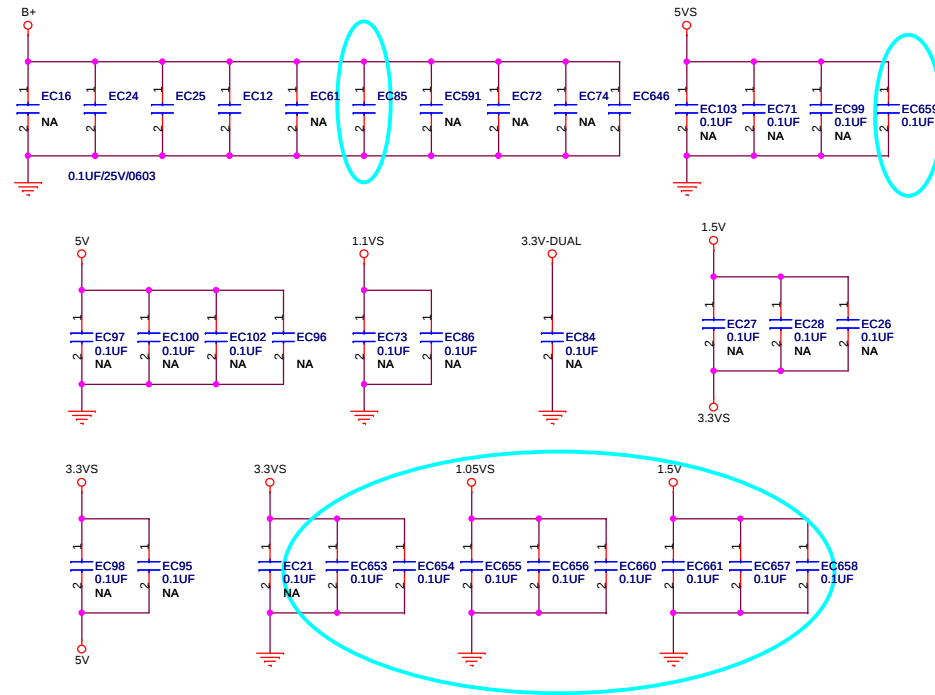
+15= 11.8V ,VG=8.11V
VGS=8.11V-3.3V=4.81V

+15= 14.6V ,VG=10.03V
VGS=10.03V-3.3V=6.73V

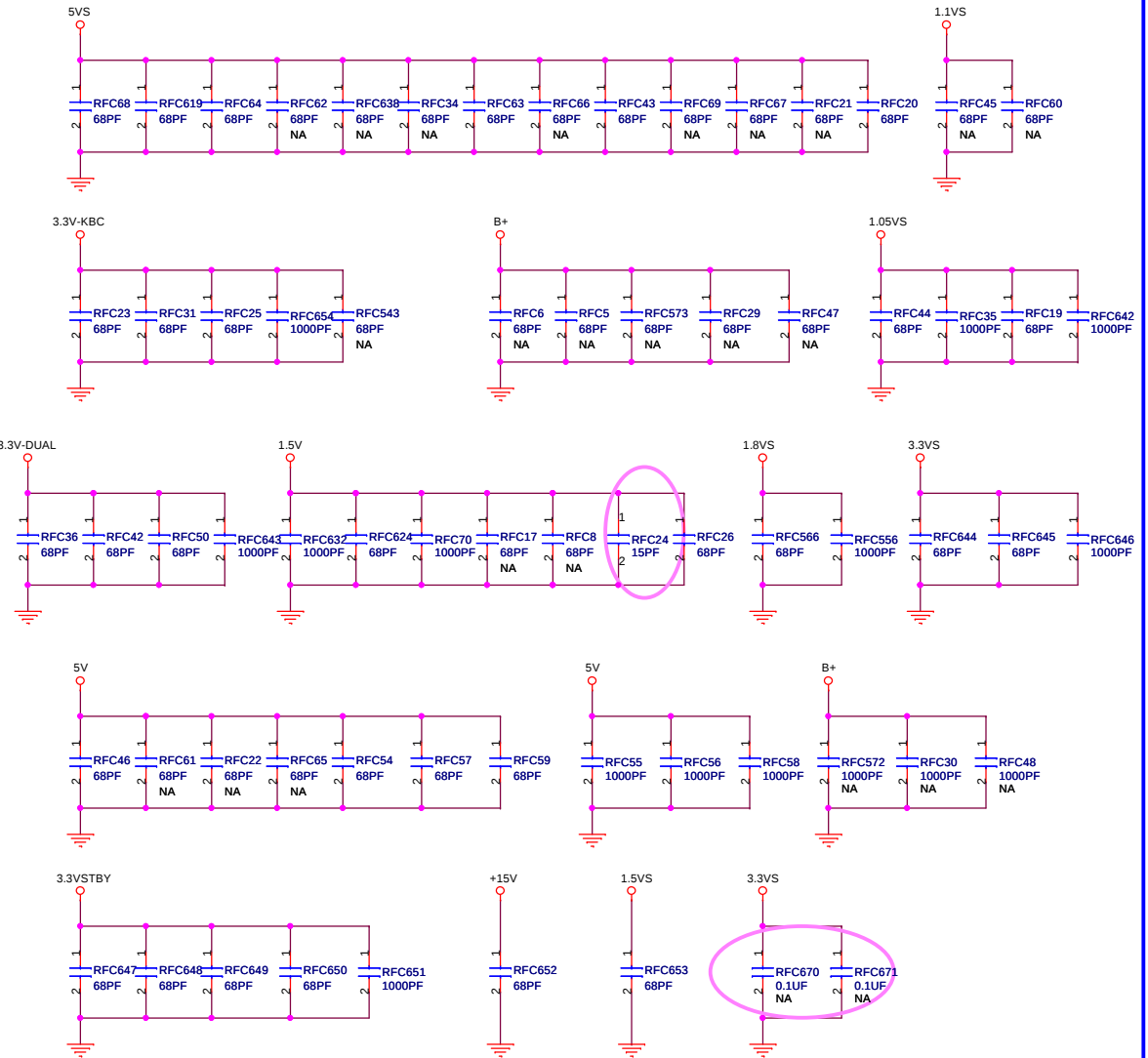




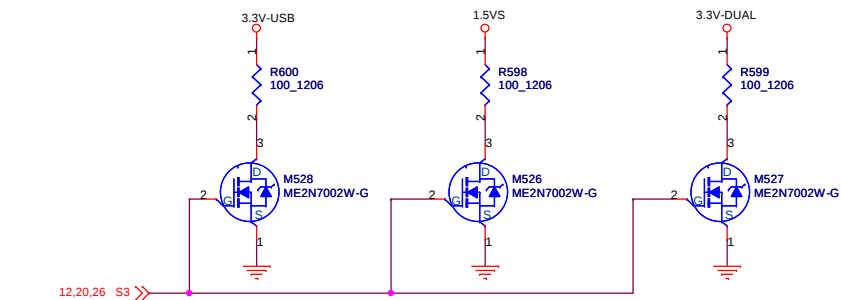
EMI Caps



RFI Caps



Discharge



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